IMPEDANCE MEASUREMENTS FOR HIGH POWER RF TRANSISTORS USING THE TRL METHOD

Impedance measurements on high power RF transistors are always a problem because of the very low values and lead widths and because the devices may be in a push-pull configuration. Calibration kits to measure wide or balanced microstrip lines are difficult to build and provide poor accuracy. This article describes a way to accurately characterize high power RF transistors, even with wide leads and in a single-ended or push-pull configuration. The impedances of the transistor or the S parameters of the input and output test fixture are obtained using the thru-reflect-line (TRL) calibration technique in order to perform de-embedding or load-pull measurements. Different options of calculation are presented.

METHOD DESCRIPTION

Generally, high power transistor characterization consists of a measurement of the optimum source and load presented to the transistor by a given test fixture. This test fixture can be tuned at each individual frequency for best performance, or included in a load-pull bench as an impedance transformer. In all cases, the impedance of the test fixture (S_{22} of the input matching network and S_{11} of the output matching network) must be measured. In the case of a load-pull, all other S_{ij} parameters must be determined in order to perform de-embedding. To determine the S parameters, a break-apart test fixture is used and included in a calibration routine with a vector network analyzer (VNA), as shown in ***Figures 1*** and **2**.

If a TRL calibration is performed instead of a short-open-load-thru (SOLT) procedure, the only standard needed is a delay line. In this case, if the delay line is designed so that it has the same width as the transistor leads, the measurement will be accurate because width transitions are avoided, as well as coaxial-to-microstrip transitions, and the measurement system will be normalized to the impedance of the delay line, which will be lower than 50 Ω if

Fig. 1 The break-apart test fixture.

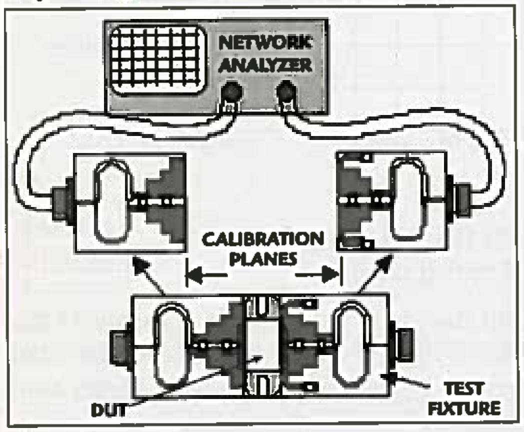
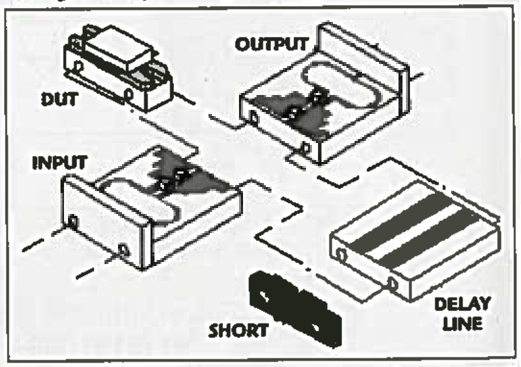


Fig. 2 Components of the test fixture.



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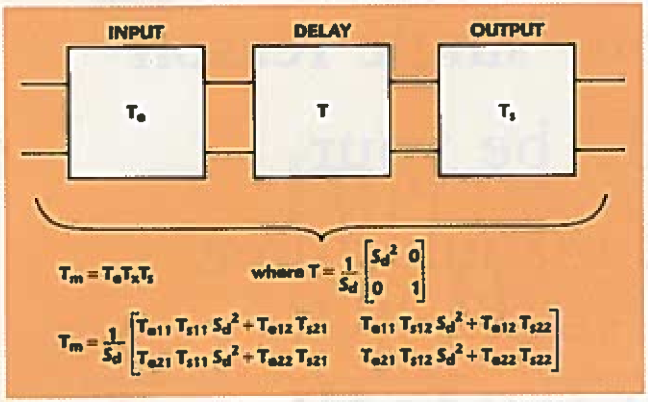
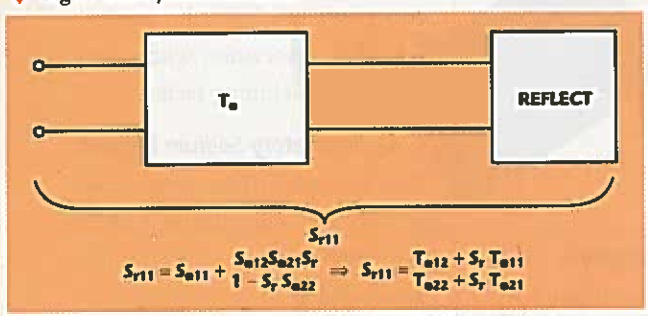
JEAN-JACQUES BOUNY
Motorola Semiconducteurs S.A.
Toulouse, France



▲ *Fig. 3 The T_m measurement.*

▼ *Fig. 4 The S_r measurement.*



the line is wide. In the case of a push-pull configuration, the delay line design is accomplished by printing two symmetric lines, making the impedance of the delay two-times the impedance of a single line. When the three measurements of the TRL calibration are completed, it is possible to calculate the error matrix corresponding to the input and output matching networks.

IMPEDANCE CALCULATION

To calculate the parameters of the error matrix, T parameters, which are cascadable, are used instead of S parameters. Translation between S and T parameters is described in ***Appendix A***. T_m is measured, as shown in ***Figure 3***, with the delay and thru to obtain T_{dij} (delay) and T_{tij} (thru) with $S_d = S_{21} = S_{12}$ of the delay line (equal to 1 in the case of the thru).

S_{rij} is subsequently measured, as shown in ***Figure 4***, where S_r is a reflecting termination (an open or short circuit). Ten relationships now exist to calculate the values of T_{eij} and T_{sij} (T parameters of the input and output test fixture, respectively) as a function of T_{dij}, T_{tij}, S_{rij}, S_r and S_d. After some mathematical calculations (detailed in ***Appendix B***), formulas are obtained where S_{s11} and S_{e22} are fully determined if S_d and S_r are presumed to be known. Note that S_d and S_r also could be calculated, however, some unknowns must be determined. For simplicity, suppose that S_d has been measured or simulated and that S_r is known (+1 for an open, or –1 for a short).

CALCULATION RESULTS

S_r and S_d now can be replaced by their values and S_{e11}, S_{ee22}, S_{s11} and S_{s22} can be obtained as functions of S_{rij}, T_{dij} and T_{tij}. $S_{e12}S_{e21}$ can be extracted from the S-parameter form of Equation A9, and the crossed term $S_{e21}S_{s21}$ can be extracted from Equation A18 knowing that it is equal to $1/T_{e22}T_{s22}$. If the input and output test fixtures are assumed reciprocal, $S_{e12} = S_{e21}$ and $S_{s12} = S_{s21}$ can be calculated as the square root of their respective products. T parameters then can be replaced by their S-parameter equivalents and the following S-parameter impedances can be obtained:

Input:

$$S_{e11} = \frac{S_{d11} S_{t21} - S_d S_{t11} S_{d21}}{S_{t21} - S_d S_{d21}}$$

$$S_{e22} = \frac{\left(S_{d11} S_{t21} - S_d S_{t11} S_{d21}\right) - S_{r11}\left(S_{t21} - S_d S_{t21}\right)}{\left(S_d S_{d11} S_{t21} - S_{t11} S_{d21}\right) - S_{r11}\left(S_d S_{t21} - S_{d21}\right)} \bullet \frac{S_d S_{t21} - S_{d21}}{S_{t21} - S_d S_{d21}}$$

$$S_{e12} S_{e21} = S_{r11}\left(1 - S_{e22}\right) - S_{e11}$$

Output:

$$S_{s11} = \frac{\left(S_{d22} S_{t21} - S_d S_{t22} S_{d21}\right) - S_{r22}\left(S_{t21} - S_d S_{d21}\right)}{\left(S_d S_{d22} S_{t21} - S_{t22} S_{d21}\right) - S_{r22}\left(S_d S_{t21} - S_{d21}\right)} \bullet \frac{S_d S_{t21} - S_{d21}}{S_{t21} - S_d S_{d21}}$$

$$S_{s22} = \frac{S_{d22} S_{t21} - S_d S_{t22} S_{d21}}{S_{t21} - S_d S_{d21}}$$

$$S_{s12} S_{s21} = S_{r22}\left(1 - S_{s11}\right) - S_{s22}$$

Crossed:

$$S_{e12} S_{s12} = S_{e21} S_{s21} = \frac{1 - S_d^2}{S_d} \bullet \frac{S_{d21} S_{t21}}{S_{t21} - S_d S_{d21}}$$

In this case, S_r is supposed to be an open; in the case of a short, the sign of S_{e22} and S_{s11} is opposite. $Z_{in}°$ and $Z_{out}°$ are given by

$$Z_{in}° = Z_o \bullet \frac{1 + S_{e22}}{1 - S_{e22}}$$

$$Z_{out}° = Z_o \bullet \frac{1 + S_{s11}}{1 - S_{s11}}$$

where Z_o is the normalization impedance of the system — the impedance of the delay line. It should be noted that the delay must be different from the thru (indeterminable if the delay is 0° or 180°), which means that the best case is when the delay is 90°. However, in a practical case, a delay line between 30° and 150° provides good accuracy.

PRACTICAL USE

Practical measurements are quite simple to implement, however, special attention must be paid to several points. First, when assembling the break-apart test fixture, the continuity of the ground must be very good. Second, if a quarter-wave delay line is used, it will transform the impe-

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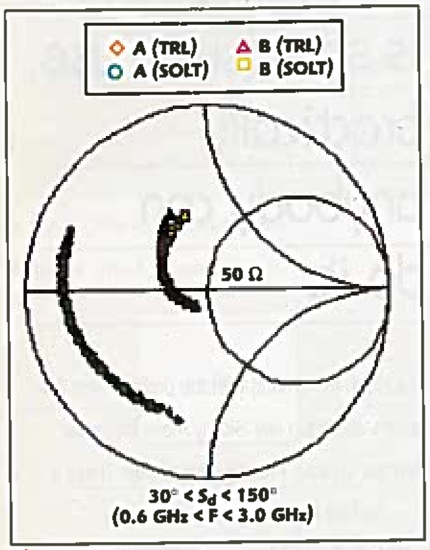
dance seen on one side (very low) to a very high impedance on the other side, and the transmitted signal will be very low. A lot of noise will be added on the measurements, and the obtained results may be unusable.



▲ *Fig. 5 SOLT and TRL measurements of the first two passive networks.*

Fig. 6 Difference between the real impedance presented to the device and that measured with a standard technique. ▼

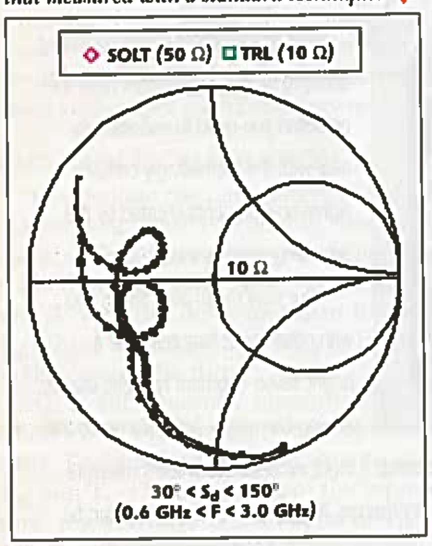


TABLE I

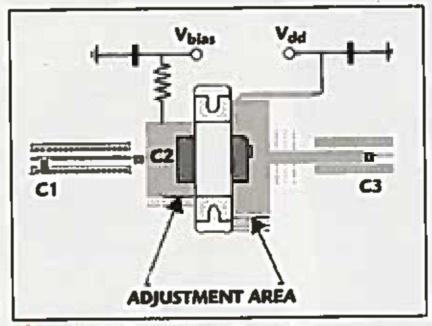
MRF18060 IMPEDANCES

Frequency (GHz)	Z_{in} (Ω)	Z_{out} (Ω)
1.70	0.60 + j2.53	2.27 + j3.44
1.80	0.80 + j3.20	2.05 + j3.05
1.90	0.92 + j3.42	1.90 + j2.90
2.00	1.07 + j3.59	1.64 + j2.88
2.10	1.31 + j4.00	1.29 + j2.99

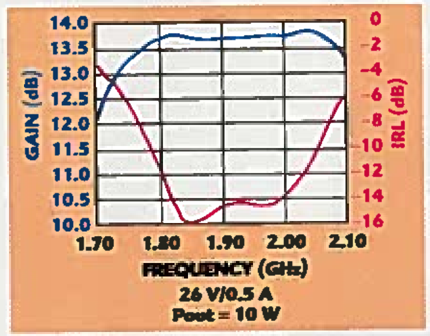
METHOD VERIFICATION

Two passive networks have been measured with a standard SOLT calibration and connector and with a TRL calibration and a 50 Ω delay line. ***Figure 5*** shows the results obtained between 0.6 and 3 GHz, which confirm that the method is valid over more than two octaves for a single delay line. Note also that even with a 50 Ω delay line, some differences exist as a result of the coaxial-to-microstrip transition.

A second set of measurements has been completed with a wide delay line (10 Ω). As shown in ***Figure 6***, there is a big difference between the real impedance presented to the device and the one measured with a standard technique.



▲ *Fig. 7 The optimized amplifier.*



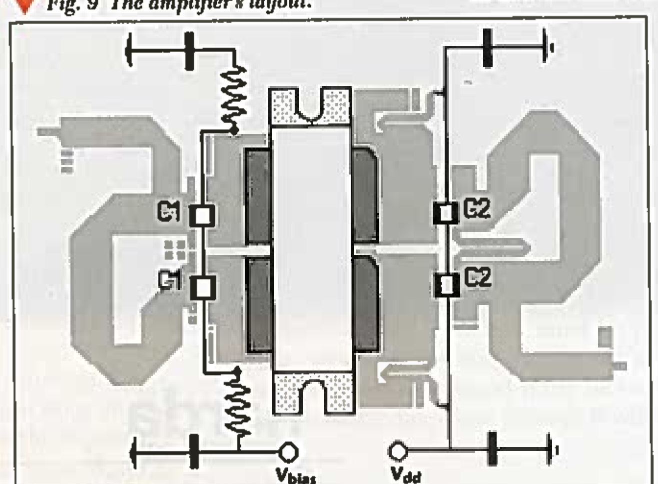
▲ *Fig. 8 The amplifier's gain and IRL vs. frequency at 10 W.*

TABLE II

MRF21120 IMPEDANCES

Frequency (GHz)	Z_{in} (Ω)	Z_{out} (Ω)
2.05	2.90 + j11.82	6.03 + j6.38
2.11	2.35 + j11.42	5.15 + j6.70
2.17	2.05 + j10.80	4.34 + j6.69
2.23	1.98 + j10.53	3.98 + j6.61

▼ *Fig. 9 The amplifier's layout.*



A DESIGN EXAMPLE

An amplifier was designed using this technique with a Motorola model MRF18060 60 W/1.8 GHz/26 V transistor. Impedances measured for 65 W and 13 dB gain at 1 dB compression are listed in ***Table 1***. A drawing of the optimized amplifier is shown in ***Figure 7***, where C1 = 1.8 pF, C2 = 1 pF and C3 = 10 pF. When the amplifier was assembled without any tuning, the results were 64 W, 12.2 dB gain and 47 percent efficiency at 1 dB compression. After adding adjustment areas at the input and output, the results became 66 W/12.7 dB gain/48.8 percent efficiency at 1.8 GHz, 67 W/12.7 dB gain/47.8 percent efficiency at 1.9 GHz and 67 W/12.8 dB gain/48.3 percent efficiency at 2.0 GHz. Gain and input return loss (IRL) are shown in ***Figure 8***.

A SECOND EXAMPLE

Another amplifier was built using a Motorola model MRF21120 120 W/2.1 GHz/26 V push-pull transistor. ***Table 2*** lists the measured impedances for 120 W/12.1 dB gain at 1 dB compression. The amplifier is shown in ***Figure 9***, where C1 = 1.8 pF and C2 = 4.7 pF. Before any tuning, the measurement results were 113 W, 11.6 dB gain and 45 percent efficiency at 1 dB compression. After a slight adjustment of the position of C1 and C2 (up and down), the results were 121

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W/12.1 dB gain/47.6 percent efficiency at 2.11 GHz and 118 W/12.1 dB gain/46.6 percent efficiency at 2.17 GHz. Gain and IRL are shown in ***Figure 10***. As in the previous example, results are very similar to those obtained when measuring the impedances in a narrow band, which demonstrates that the method is valid and accurate.

For designers with access to a VNA with TRL calibration capability, an alternative solution consists of using the internal calibration routine of the VNA and extracting the error parameters corresponding to S_{eij} and S_{sij}. In this case, the calibration can be verified by measuring the thru.

A NONINSERTABLE QUADRIPOLE

When a de-embedding solution is required, all parameters can be calculated with the presented method. However, a first calibration must be completed in the connector plane before the measurements are performed. The VNA routine also may be used and two successive calibrations performed: one in the connector plane (cal 1, error matrix M), and a second one (TRL) including the test fixture (cal 2, error matrix N). By using T parameters, the X_{ij} (S_{ij} parameters of the test fixture) may be calculated, as shown in ***Figure 11***.

After some algebra, the input or output becomes

$$X_{11} = \frac{N_{11} - M_{11}}{M_{22}N_{11} - \Delta M}$$

$$X_{12} = \frac{M_{21}N_{12}}{M_{22}N_{11} - \Delta M}$$

$$X_{21} = \frac{M_{12}N_{21}}{M_{22}N_{11} - \Delta M}$$

$$X_{22} = \frac{M_{22}\Delta N - N_{22}\Delta M}{M_{22}N_{11} - \Delta M}$$

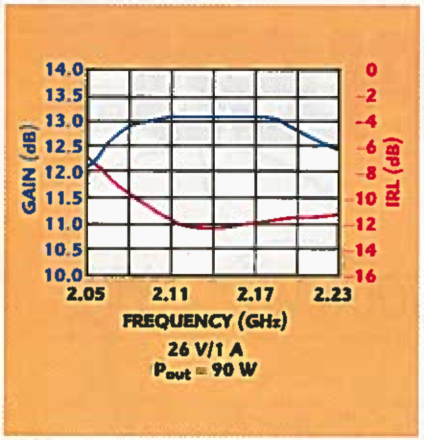
In a calibration set, S_{12} and S_{21} of the different error matrices are not known independently; however, $X_{12}X_{21}$ can be calculated as a function of $M_{12}M_{21}$ and $N_{12}N_{21}$. If the quadripole is assumed reciprocal, that value is equal to X_{21}^2 and X_{12}^2 such that

$$X_{12} = X_{21} = \pm\frac{\sqrt{(M_{12}M_{21})\bullet(N_{12}N_{21})}}{M_{22}N_{11} - \Delta M}$$

The sign then must be determined using an approximate value of X_{21}.

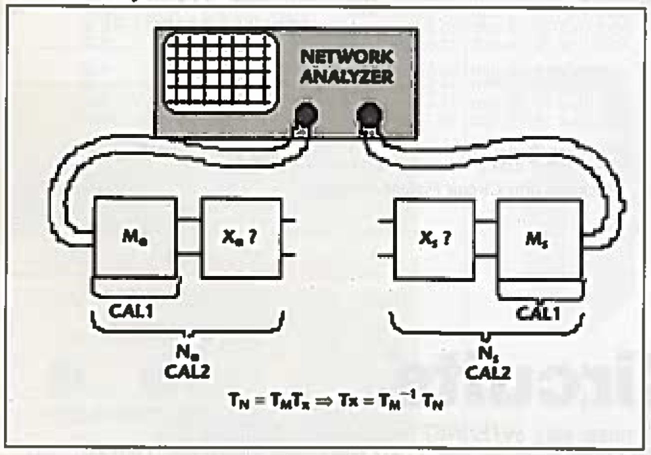
CONCLUSION

It has shown that the TRL calibration technique can provide precise characterization of high power RF transistors, including impedances and board measurements for de-embedding. Examples show that this technique is much more accurate than standard techniques using coaxial SOLT calibration because measurements are done without any coaxial-to-microstrip transition or width transition and can be performed in a low impedance system. The only calibration standard required to be built is a delay line that can be used over more than two octaves. The use of the TRL method for impedance measurement allows the designer to build an optimized amplifier at the first pass, which drastically reduces the design's cost and cycle time. ■



▲ *Fig. 10 The amplifier's gain and IRL vs. frequency at 90 W.*

▼ *Fig. 11 X_{ij} determination.*



APPENDIX A

S and T Parameters

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = [S]\bullet\begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

$$\begin{pmatrix} b_1 \\ a_1 \end{pmatrix} = [T]\bullet\begin{pmatrix} a_2 \\ b_2 \end{pmatrix}$$

where

$$[S] = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

$$[T] = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix}$$

Figure A1 shows the parameter orientations.

S to T Translation

$$[T] = \frac{1}{S_{21}}\begin{pmatrix} -\Delta S & S_{11} \\ -S_{22} & 1 \end{pmatrix}$$

where

$\Delta S = S_{11}S_{12} - S_{12}S_{21}$

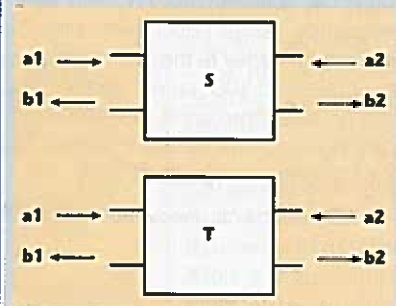
It should be noted that the expression for T_{11} as a function of S parameters is more complex than for T_{12}, T_{21} and T_{22}. For this reason, when there is a choice between two expressions, the one that does not contain T_{11} is chosen.

T to S Translation

$$[S] = \begin{pmatrix} \frac{T_{12}}{T_{22}} & \Delta T \\ \frac{1}{T_{22}} & -\frac{T_{21}}{T_{22}} \end{pmatrix}$$

where

$\Delta T = T_{11}T_{22} - T_{12}T_{21}$



▲ *Fig. A1 S and T relationships.*

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APPENDIX B

Calculation Details

First, the 10 relations given by the measurements are

delay

$$S_dT_{d11} = T_{e11}T_{s11}S_d^2 + T_{e12}T_{s21} \quad (A1)$$

$$S_dT_{d12} = T_{e11}T_{s12}S_d^2 + T_{e12}T_{s22} \quad (A2)$$

$$S_dT_{d21} = T_{e21}T_{s11}S_d^2 + T_{e22}T_{s21} \quad (A3)$$

$$S_dT_{d22} = T_{e21}T_{s12}S_d^2 + T_{e22}T_{s22} \quad (A4)$$

thru

$$T_{t11} = T_{e11}T_{s11} + T_{e12}T_{s21} \quad (A5)$$

$$T_{t12} = T_{e11}T_{s12} + T_{e12}T_{s22} \quad (A6)$$

$$T_{t21} = T_{e21}T_{s11} + T_{e22}T_{s21} \quad (A7)$$

$$T_{t22} = T_{e21}T_{s12} + T_{e22}T_{s22} \quad (A8)$$

reflect

$$S_{r11} = \frac{T_{e12}+S_rT_{e11}}{T_{e22}+S_rT_{e21}} \quad (A9)$$

$$S_{r22} = \frac{-T_{s21}+S_rT_{s11}}{-T_{s22}+S_rT_{e12}} \quad (A10)$$

In addition, it is known that $S_{e22} = -T_{e21}/T_{e22}$ yields Z_{in}^* (conjugate of the transistor's input impedance), and $S_{s11} = +T_{s12}/T_{s22}$ produces Z_{out}^*.

Equations A11 to A20 are obtained by making some combinations between Equations A1 to A10 (for example, Equation A1 – Equation A5, Equation A1 – (S_d^2) Equation A5, Equation A2 – Equation A6, Equation A2 – (S_d^2) Equation A6, producing

$$S_dT_{d11} - T_{t11} = T_{e11}T_{s11}(S_d^2-1) \quad (A11)$$

$$S_dT_{d12} - T_{t12} = T_{e11}T_{s12}(S_d^2-1) \quad (A12)$$

$$S_dT_{d21} - T_{t21} = T_{e21}T_{s11}(S_d^2-1) \quad (A13)$$

$$S_dT_{d22} - T_{t22} = T_{e21}T_{s12}(S_d^2-1) \quad (A14)$$

$$S_dT_{d11} - S_d^2T_{t11} = T_{e12}T_{s21}(1-S_d^2) \quad (A15)$$

$$S_dT_{d12} - S_d^2T_{t12} = T_{e12}T_{s22}(1-S_d^2) \quad (A16)$$

$$S_dT_{d21} - S_d^2T_{t21} = T_{e22}T_{s21}(1-S_d^2) \quad (A17)$$

$$S_dT_{d22} - S_d^2T_{t22} = T_{e22}T_{s22}(1-S_d^2) \quad (A18)$$

$$S_{r11}\left(1+S_r\frac{T_{e21}}{T_{e22}}\right) = \frac{T_{e12}}{T_{e22}} + S_r\frac{T_{e11}}{T_{e22}} \quad (A19)$$

$$S_{r22}\left(-1+S_r\frac{T_{s12}}{T_{s22}}\right) = -\frac{T_{s21}}{T_{s22}} + S_r\frac{T_{s11}}{T_{s22}} \quad (A20)$$

Concerning the input, dividing Equation A15 by Equation A17 or Equation A16 by Equation A18, and Equation A11 by Equation A13 or Equation A12 by Equation A14 yields

$$\frac{T_{e12}}{T_{e22}} = \frac{T_{d11}-S_dT_{t11}}{T_{d21}-S_dT_{t21}} = \frac{T_{d12}-S_dT_{t12}}{T_{d22}-S_dT_{t22}}$$

$$\frac{T_{e11}}{T_{e21}} = \frac{S_dT_{d11}-T_{t11}}{S_dT_{d21}-T_{t21}} = \frac{S_dT_{d12}-T_{t12}}{S_dT_{d22}-T_{t22}} \quad (A21)$$

$$\Rightarrow \frac{T_{e11}}{T_{e22}} = \frac{S_dT_{d11}-T_{t11}}{S_dT_{d21}-T_{t21}} \bullet \frac{T_{e21}}{T_{e22}} = \frac{S_dT_{d12}-T_{t12}}{S_dT_{d22}-T_{t22}} \quad (A22)$$

Note that $S_{e11} = T_{e12}/T_{e22}$ is now calculated. These results are used in Equation A19 to obtain

$$S_r\frac{T_{e21}}{T_{e22}}\left(S_{r11}-\frac{S_dT_{d12}-T_{t12}}{S_dT_{d22}-T_{t22}}\right) = \frac{T_{d12}-S_dT_{t12}}{T_{d22}-S_dT_{t22}} - S_{r11} \quad (A23)$$

S_{e22} is now fully determined if it is assumed that S_d and S_r are known (same for S_{e11}). Applying the same method to the output yields

$$S_r\frac{T_{s12}}{T_{s22}}\left(S_{r22}-\frac{S_dT_{d21}-T_{t21}}{S_dT_{d22}-T_{t22}}\right) = -\frac{T_{d21}-S_dT_{t21}}{T_{d22}-S_dT_{t22}} + S_{r22} \quad (A24)$$

where S_{s11} and S_{s22} are fully determined if S_d and S_r are known.

S_d Calculation

Equation A21 is used to extract S_d, and the second-order equation becomes

$$S_d^2(T_{t11}T_{t22} - T_{t12}T_{t21}) + S_d \bullet (T_{d21}T_{t12} + T_{d12}T_{t21} - T_{d11}T_{t22} - T_{d22}T_{t11}) + (T_{d11}T_{d22} - T_{d12}T_{d21}) = 0$$

Only an indetermination remains to be solved (which root to choose) to obtain the value of S_d.

S_r Calculation

In fact, S_r will not be calculated, but a way to extract S_{e22} and S_{s11} without knowing it will be determined. By dividing Equation A23 by Equation A24 to obtain S_{e22}/S_{s11} (= A) and dividing Equation A14 by Equation A18 to obtain $S_{e22} \times S_{s11}$ (= B), S_{e22} and S_{s11} are now calculated as

$$S_{e22} = \pm\sqrt{AB} \qquad S_{s11} = \pm\sqrt{\frac{A}{B}}$$

As before, the indetermination of the sign of the square root must be solved.