What's New in ADS 2006A

"Start Closer to the Finish Line"

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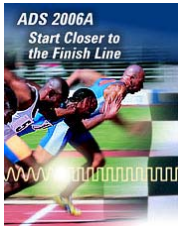
ADS 2006A Release at a Glance

New

- ✓ ✪ RF Architecture tools for ADS
  - GENESYS Synthesis
  - GENESYS Spectrasys
  - GENESYS WhatIF
- ✓ Embedded Knowledge Search
- ✪ 5 New Wireless Libraries
- ✪ Connected Solution Workbench
- Device and Behavioral models
- ✪ *Coming in winter 2006-2007: features for Signal Integrity (SI)*

Improved

- 64-bit simulators
- HB for frequency dividers
- Transient & Convolution speed-up
- Ptolemy simulation scheduler, imports & exports
- Momentum 3D Via currents
- Data Display peak markers
- Enhanced flows & translators
- Layout performance gains
- Downloadable SMT Libraries



✓ *These key features help you "Start Closer to the Finish Line"*

✪ *These key features involve new products*

What's New in 2006 for ADS and RFDE

"Start Closer to the Finish Line"

1. **New Technology**
   solves new problems and
   gives you a design advantage
2. **Extended Performance & Accuracy**
   conquer existing problems so
   you are confident that designs
   will work the first time.
3. **Accessibility & Flow Integration**
   within your Design Flow puts Agilent
   tools closer to the design problems
4. **Usability and Quality**
   frees your creativity and makes the most of your effort

New Technology in 2006

- Solves new challenges
- "***Start your design closer to the finish line***"

Frequency Planning

RF System Architecture

Circuit Synthesis & Simulation Assistance

Robust Spice Models

New Technology in ADS 2006

Frequency Planning

– Unique architecture product helps you avoid spurs and interference in RF systems, saving days or weeks with manual spreadsheets and charts.

RF System Architecture

– Make better architecture & component choices. Avoid expensive changes late in the design process. Unique simulator helps you find the “smoking gun” early, and begin implementation, with live links to ADS

Circuit Synthesis & Simulation Assistance

– New modules for circuit synthesis and simulation assistance give you a head start on your implementation in ADS

Robust Spice Models

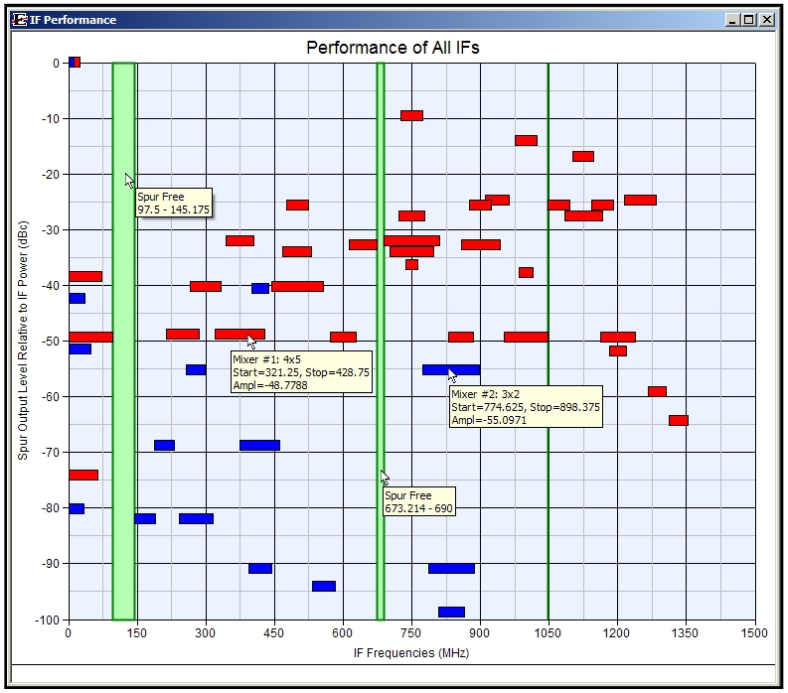
– New models for active devices, and advanced modeling technology for passive structures, allow for fast, accurate simulation of emerging designs

Introducing: the "WhatIF" simulator for RF frequency planning

Synthesize spur-free Intermediate Frequency (IF) bands. Avoid discovering topology limitations late in your implementation.

WhatIF

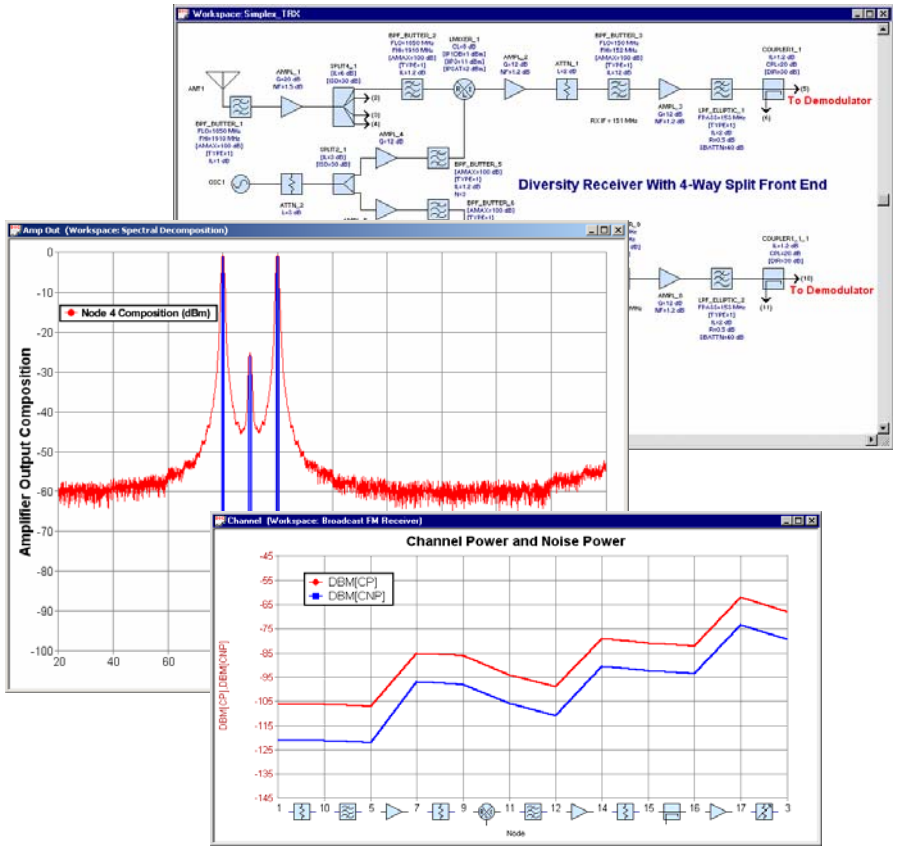
- Displays spur-free frequency bands in an easy-to-read chart
- Easily diagnose the origin of unwanted spectrum lines
- Explore topologies and qualitative specifications
- Accounts for spurs and electrical details that spreadsheets always miss



Cuts days/weeks of spreadsheet analysis down to hours!

Introducing: "Spectrasys"
Continuous spectrum simulation with SPARCA

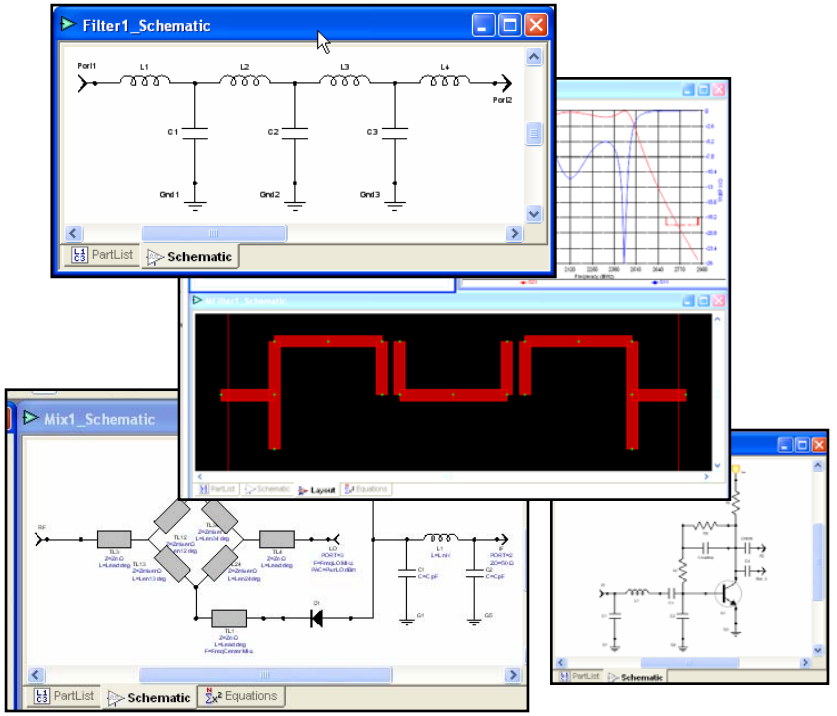
- Industry's first continuous spectrum simulator. DC-to-daylight spectrum at every node.
- Unique "Spectral Propagation and Root Cause Analysis" (SPARCA)
- Goes beyond "budget" tools and spreadsheets to help you fix RF Architecture problems that other methods never find
  - Easy to use
  - Flexible and interactive
  - Exports common RF block diagrams directly to ADS



Complements existing "bottom-up" design verification tools in ADS

Introducing:
Eagleware's Synthesis modules for ADS

- 8 Synthesis tools from Eagleware packaged for use with ADS:
  - S/FILTER (M/FILTER + FILTER)
  - A/FILTER
  - EQUALIZE
  - MATCH
  - Advanced Transmission Line
  - SIGNAL CONTROL
  - OSCILLATOR
  - MIXER
- Export your design directly to ADS
  - Thousands sold, individually

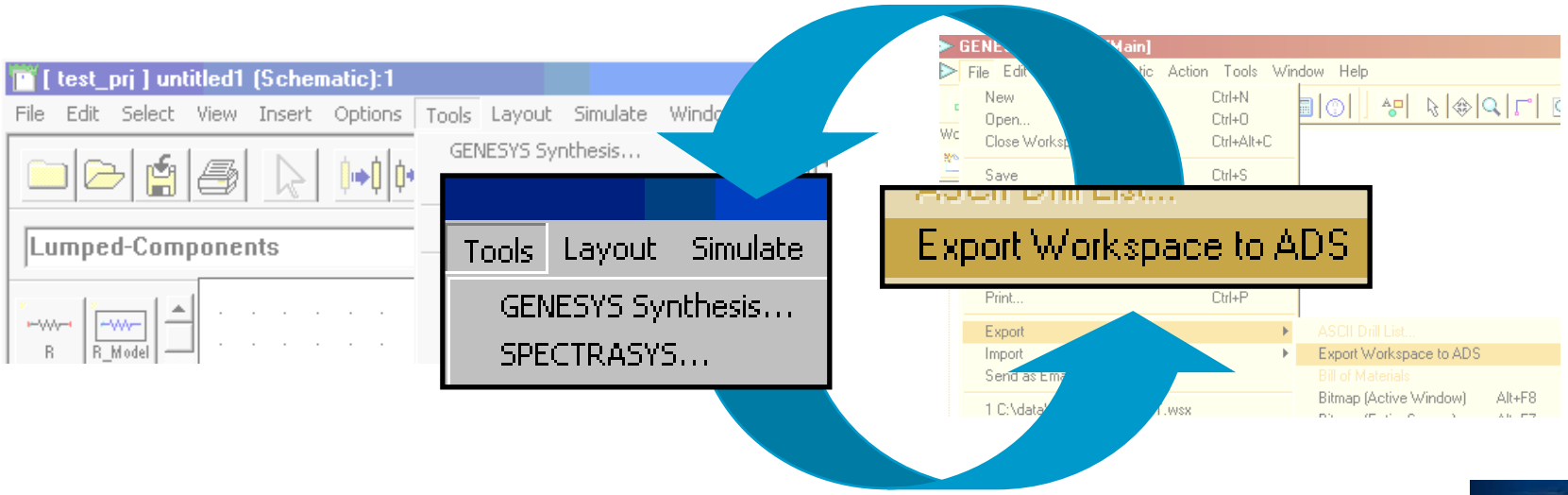


Start closer to a finished design in ADS with Genesys Synthesis

How can ADS Users access these new tools?

New GENESYS add-on packages for ADS users

- Invoke the unique GENESYS tools from your ADS session
- Transfer schematics back to ADS when you're done (real time!)
- Streamlined licensing, compatible with ADS



All these products help you "start closer to the finish line"

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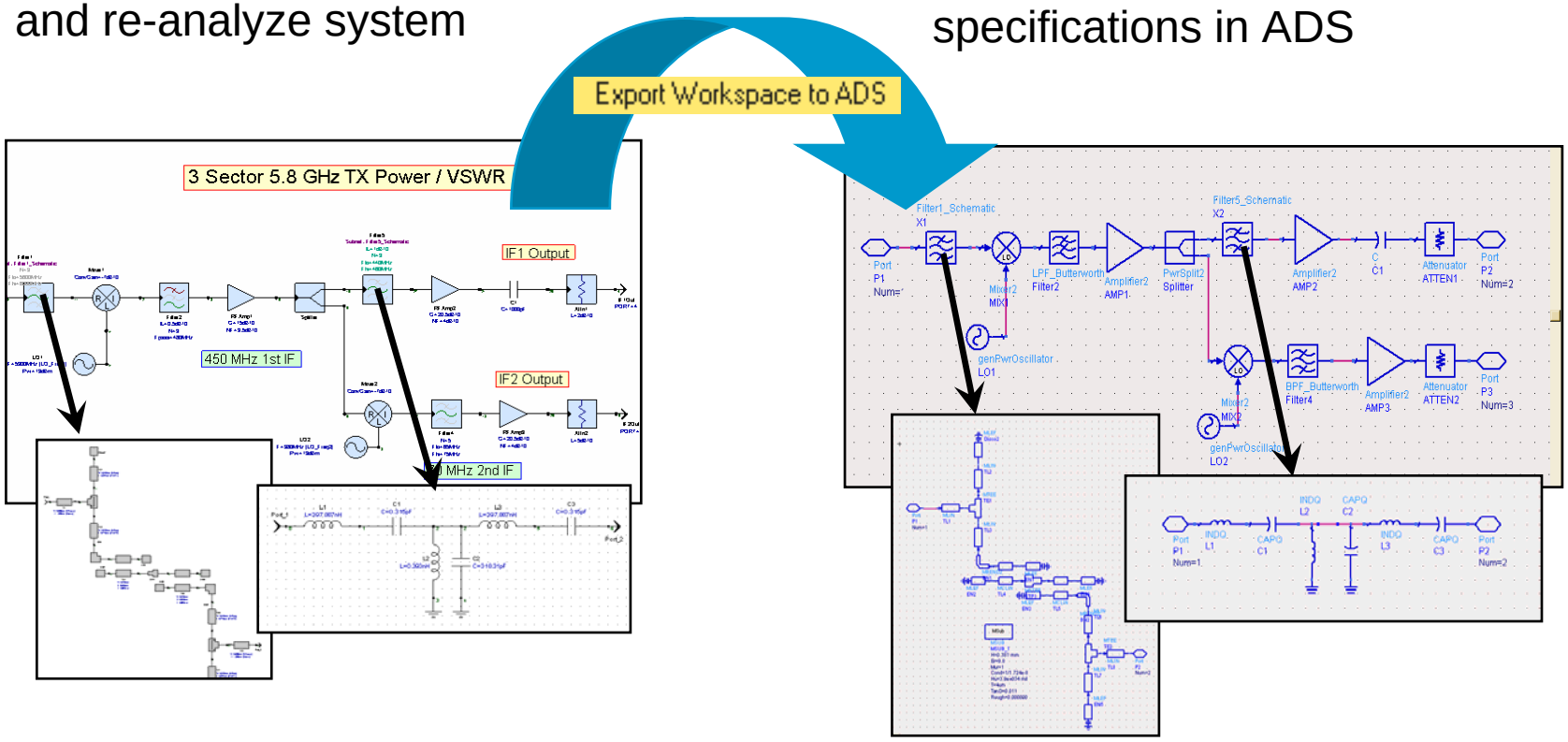
Start interactively in GENESYS, Finish in your established ADS design flow

1. Evaluate RF system architecture
2. Synthesize lower level components and re-analyze system
3. Transfer design hierarchy to ADS
4. Finish design & verify system specifications in ADS



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How can ADS Users access these new tools?

- Easily administered alongside normal ADS licenses:

If GENESYS sees this new license...

```
INCREMENT ads_rf_architect agileesofd 2.6 27-apr
```

...Then GENESYS re-uses these ADS licenses for its own environment as needed,

```
INCREMENT ads_schematic   agileesofd 2.6 27-apr-
INCREMENT ads_datadisplay agileesofd 2.6 27-apr-
INCREMENT sim_linear      agileesofd 2.6 27-apr-
INCREMENT ads_layout      agileesofd 2.6 27-apr-
```

...and unlocks unique, additional capabilities.

```
genesys_synthesis (several synth tools)
genesys_whatif
genesys_spectrasys
```

Software Release	Can re-use ADS schematic license	Expanded IFF support	Live transfers GEN → ADS
GEN 2005.11	standalone only		
GEN 2006.04	X		
GEN 2006.07	X	X	
GEN 2006.10	X	X	X
ADS 2005A	n/a	*	
ADS 2006A	n/a	X	X

** 2005A requires a Schematic IFF Translator license, which is no longer required in 2006A*

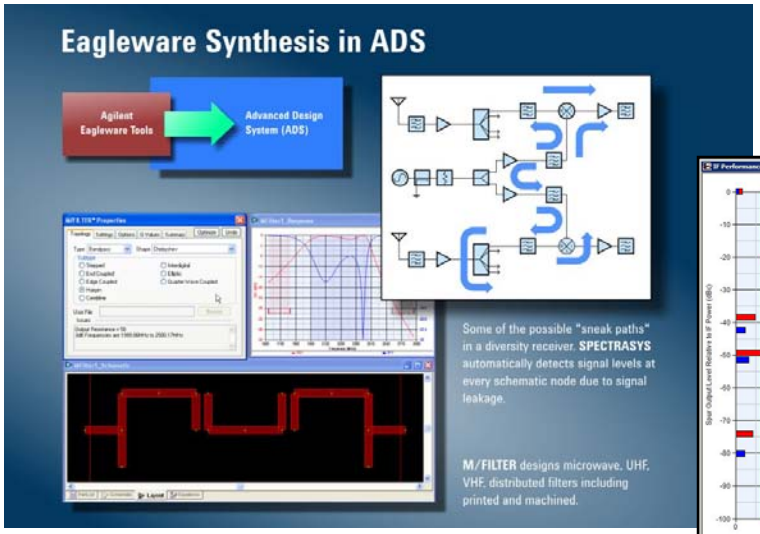
A choice of GENESYS Add-ons for ADS users

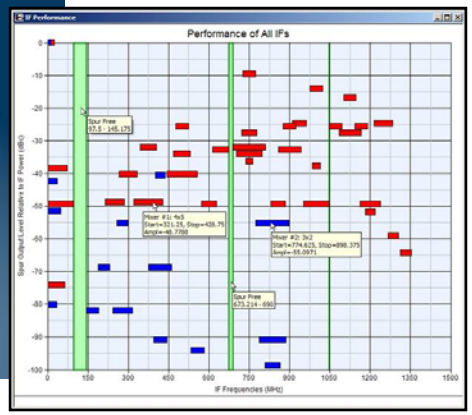
W1421
"GENESYS Synthesis for ADS"

- Includes **all 8 Synthesis tools** at an attractive price, and re-uses your ADS front-end licenses

W1422
"RF Architect for ADS"

- Includes **all 8 Synthesis tools**.
- Includes **Spectrasys**, a unique tool for root-cause spur analysis, and RF budget & system analysis.
- Includes **WhatIF**, a unique tool for RF frequency planning.





Common licensing with ADS

Introducing: 5 New Wireless Libraries for Ptolemy

- E8887 HSPA Wireless Library
- E8871 802.11n Wireless Library
- E8870 Fixed WiMax Wireless Library (802.16d)
- E8869 Mobile WiMax Wireless Library (802.16e)
- E8933 WiMedia Wireless Library (*replaces E8872 UWB Wireless Library*)

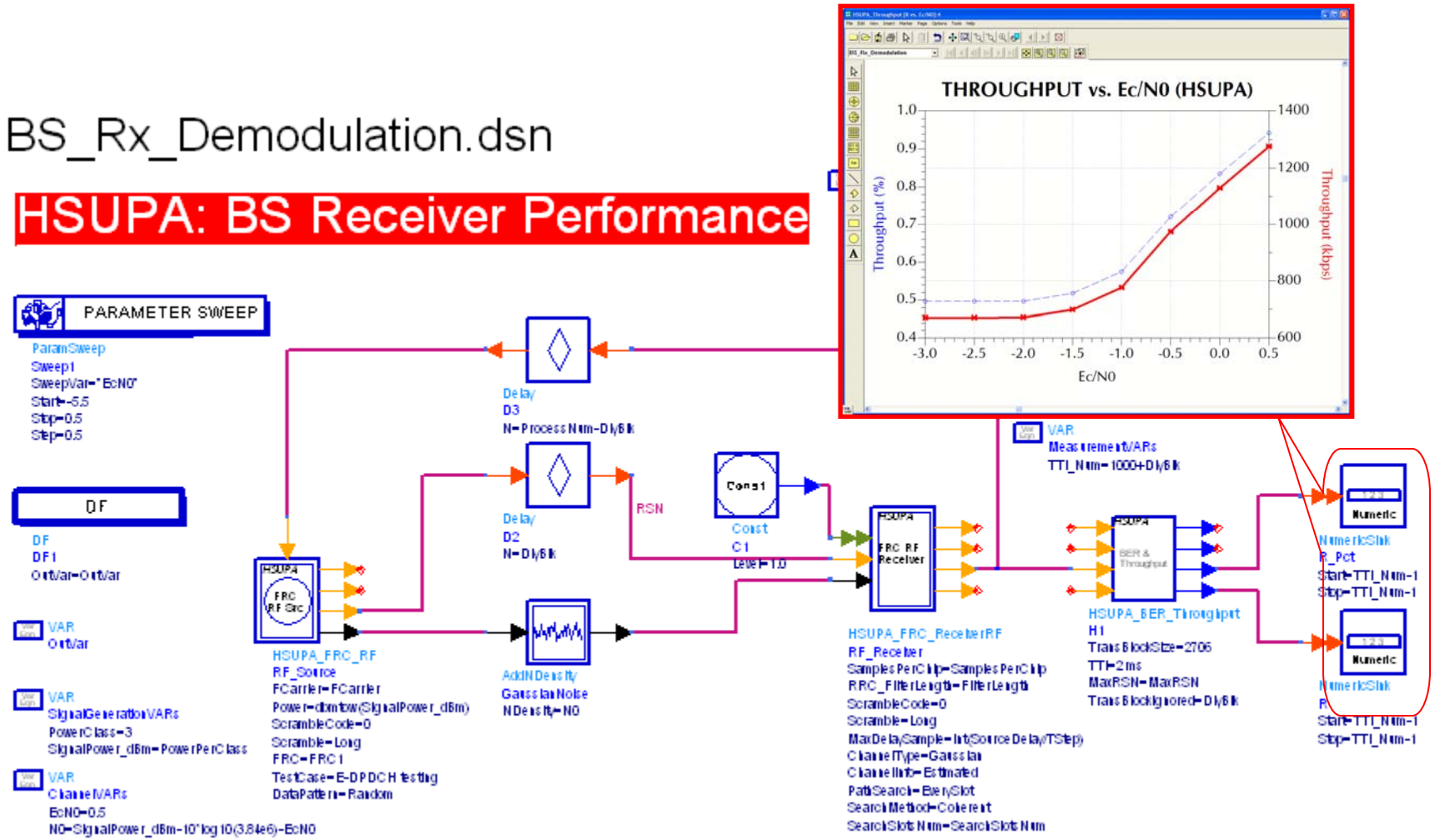
Each comes with:

- Function blocks that faithfully implement each wireless standard
- Algorithms that are consistent with Agilent measurement equipment
- Stimulus/response test benches, as described by the std's committees
- Ability to download to Sig Gen's, and upload from VSA's, and more
- Documentation and support

ADS now has **15** such wireless libraries for standards-based Cellular, Networking, and DTV design!

Example: E8887 HSPA Wireless Library

Study of effective data throughput (kb/s) vs. noise level, with RF effects



Example: E8869 Mobile WiMax Wireless Library

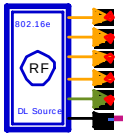
Demod a Ptolemy simulation with a VSA – true standards interoperability

WMAN_OFDMA_DL_VSA.dsn

WMAN OFDMA : Downlink Transmitter connected with 89600

WMAN_OFDMA_DL_VSA_Info
Information

Push into Info to read local information



WMAN_M_DL_SignalSrc_RF
DL_Source

FCarrier=FCarrier
Power=SignalPower
Bandwidth=Bandwidth
OversamplingOption=OversamplingOption
FFTSize=FFTSize
CyclicPrefix=CyclicPrefix
FrameMode=FDD
DL_Ratio=0.5
FrameDuration=FrameDuration
DLMAP_Enable=YES
ULMAP_Enable=YES
PreambleIndex=PreambleIndex
FrameNumber=FrameNumber
DL_PermBase=DL_PermBase
DCD_Count=1

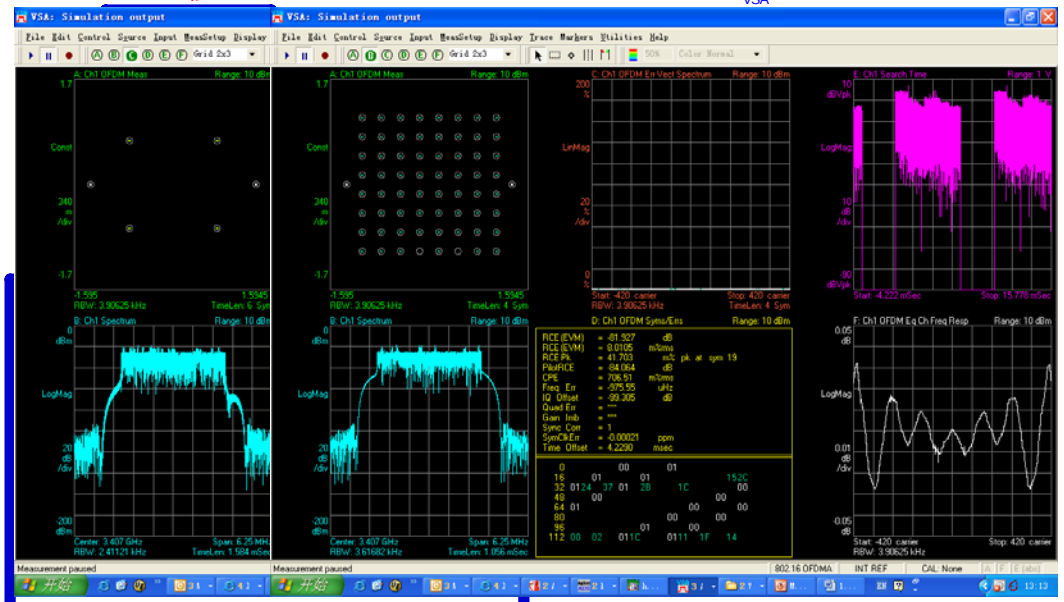
AutoMACHeaderSetting=NO
CRC32_Mode=MSB first
ZoneType=ZoneType
NumberOfBurst=NumberOfBurst
BurstWithFEC=BurstWithFEC
DataLength=DataLength
CodingType=CodingType
Rate_ID=Rate_ID
RepetitionCoding=RepetitionCoding
PowerBoosting=PowerBoosting

VSA_89600_1_Sink
VSA

VAR
DL_Case1_Params

CodingType={0,0,0}
FrameDuration=5
NumberOfBurst=3
FFTSize=1
ZoneType=0
ZoneNumOfSym=24
GroupBitmask={1,1,1,1,1,1}
BurstWithFEC=1
DataLength={1,1,1}
BurstSymOffset={2,10,16}
BurstSubchOffset={11,2,17}
BurstNumOfSym={6,6,4}
BurstNumOfSubch={5,10,2}
Rate_ID={1,2,4}
RepetitionCoding={0,0,0}

PowerBoosting={0,0,0}
PreambleIndex=2
FrameIncreased=0
DL_PermBase=12
PRBS_ID=0
OversamplingOption=1
FrameNumber=0
Bandwidth=3.5MHz
CyclicPrefix=1/32
FCarrier=3407MHz
SignalPower=dbmtow(0)



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E8933 WiMedia Wireless Library Test Benches

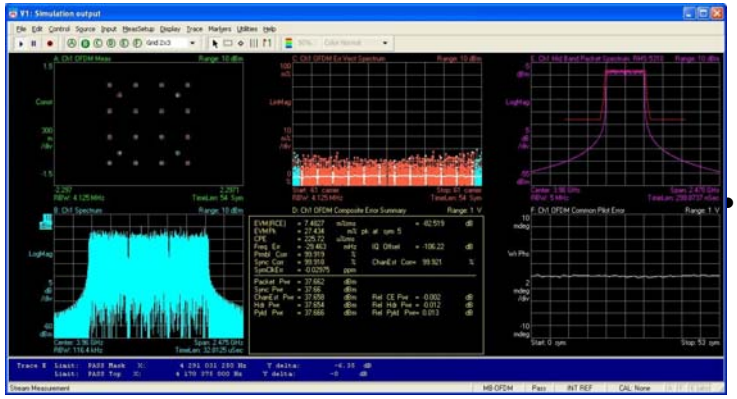
Established, standards-based tests to facilitate verification

Tx Measurement

- EVM,
- Constellation,
- CCDF
- Spectrum Mask
- Waveform

Rx Measurement

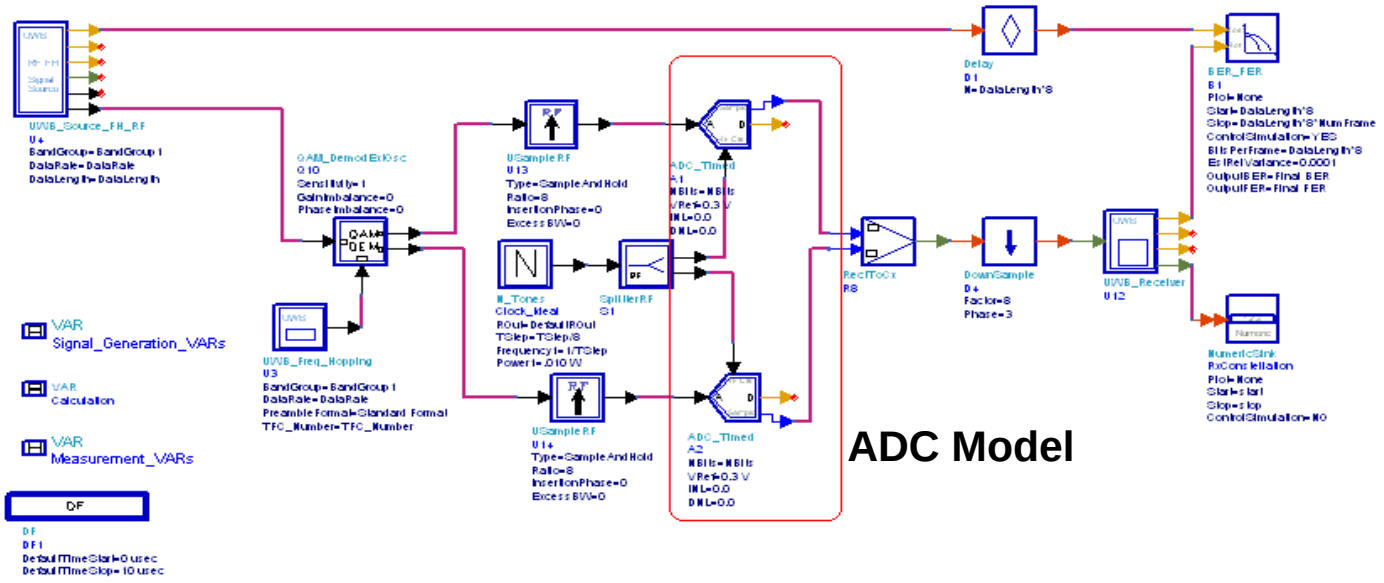
- Receiver Sensitivity
- PER vs Range in AWGN

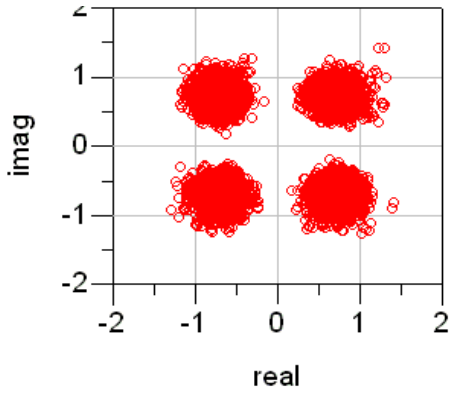


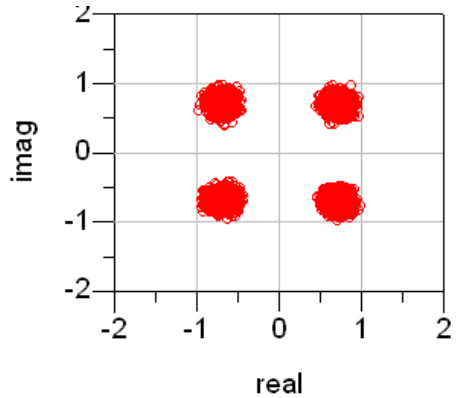
Test benches in three projects:

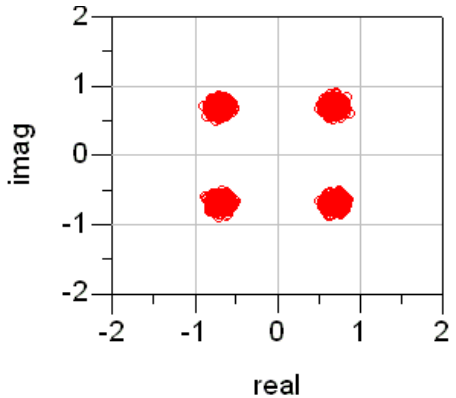
- UWB MB-OFDM TX testbenches
  - UWB_OFDM_TxCCDF.dsn,
  - UWB_OFDM_TxEVM.dsn,
  - UWB_OFDM_TxSpectrum.dsn
  - UWB_OFDM_ADC_Effect.dsn ***NEW***
  - UWB_OFDM_Demo.dsn
- UWB MB-OFDM RX testbenches
  - UWB_OFDM_RxSensitivity.dsn
  - UWB_OFDM_PER_vs_Range_AWGN.dsn
  - UWB_OFDM_Rx_with_WLAN_11a_Interferer.dsn ***NEW***
  - UWB_OFDM_Rx_with_WiMax_interferer.dsn ***NEW***
- UWB MB-OFDM RF verification testbenches
  - UWB_Tx_test.dsn
  - UWB_RX_sensitivity_test.dsn
  - UWB_RX_with_WLAN_11a_interferer_test.dsn ***NEW***

Example: E8933 WiMedia ADC quantization error









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New Technology in 2006: models

- New models supported in ADS 2006A
  - BSIM 4.5, BSIM 3v3.3, PSP
  - PIN and SRD (step-recovery) diodes
  - IMT-based Mixer
    - Adds simulation-based data extractors to convert physical designs into fast, multi-dimensonal, data-based behavioral models
  - Included with support updates at no charge

E4687 Broadband SPICE Model Generator

(new product, available ADS 2006 Update Release 1)

Ideal for

1. Users of time-domain simulators
   - ADS/RFDE modules: E8884 Transient, E8885 Convolution
   - Any SPICE simulator used for high-frequencies, or fast edge rates
2. Who also use frequency-domain S-parameter data produced by
   - EM simulators, such as Momentum (2.5D) or EMDS (3D)
   - Physical models
   - Vector Network Analyzers

Typical applications:

- RFIC: data for spiral inductors, IC packages, DUT boards
- Signal integrity and high-speed interconnect applications
- Wideband physical structures, and connectors

E4687 Broadband SPICE Model Generator

What it does:

1. Takes in frequency-domain S/Y/Z-parameters
2. Conditions data to be passive and causal for use in the time-domain
3. Outputs a fast, well-behaved SPICE equivalent circuit
   - Berkeley Spice 2G6 & 3, rational polynomials, and other native formats

Watch for several significant enhancements in ADS for Signal Integrity applications in 2006-7

Extended Performance and Accuracy in 2006

- Conquers existing problems faster and more effectively
- Gives you confidence that your design will work right, the first time.

Simulator improvements

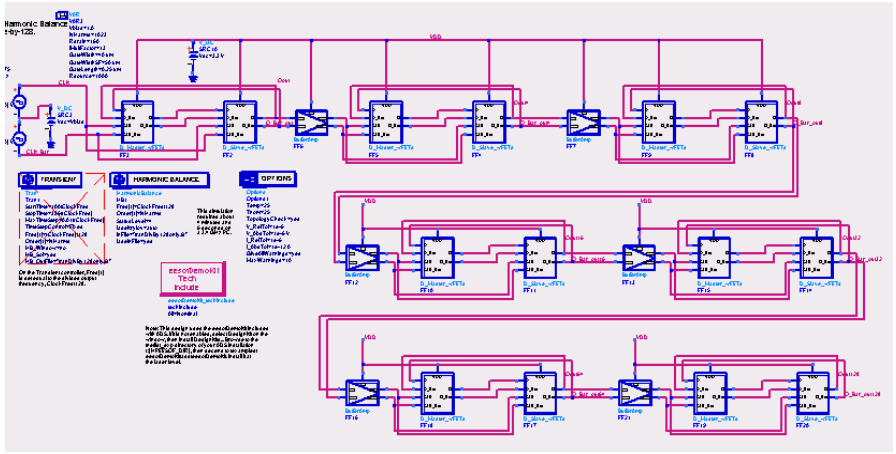
64-bit OS support

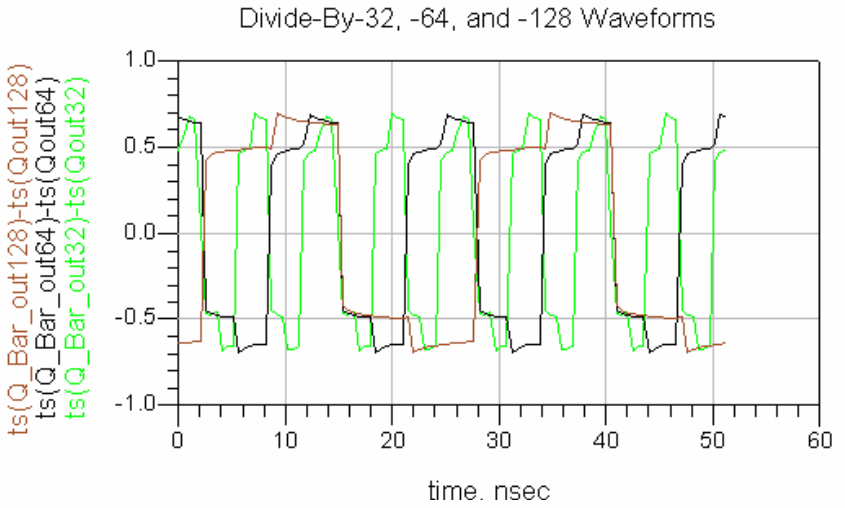
Other core improvements to PDE, Data Display, Layout, Simulators

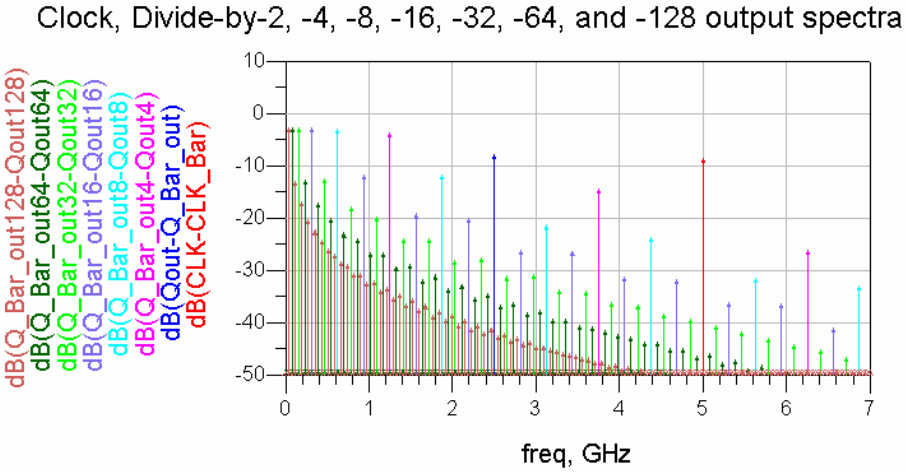
Harmonic Balance simulation

Enhancements for Frequency Dividers (released Feb. 2006)

- Enhanced convergence on difficult RFIC frequency dividers
- Divide ratios up to 32 shown in real circuits, up to 1024 observed







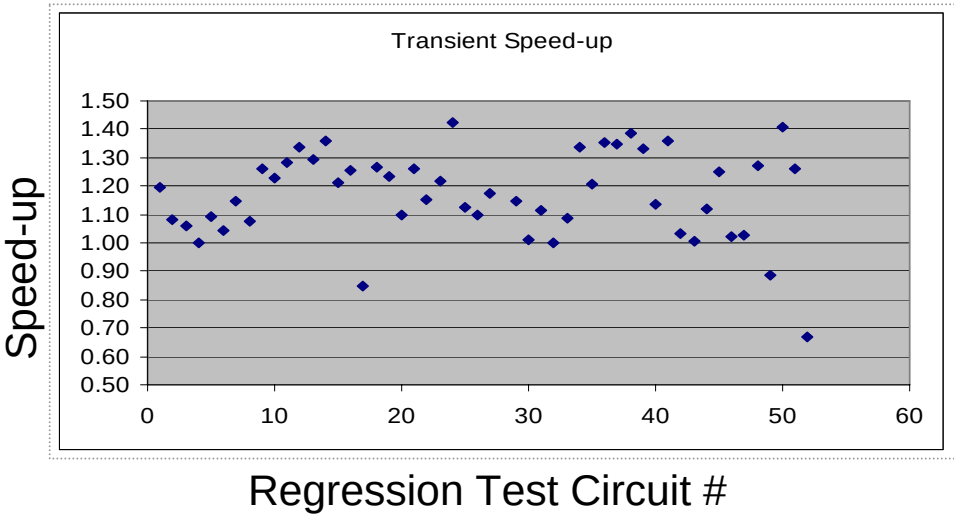
Transient simulation

Improved Raw Speed and Convergence for 2006A

Updated Transient simulator

- Algorithmic improvements
- Device optimization
- Code optimization

• +30% raw speed improvement



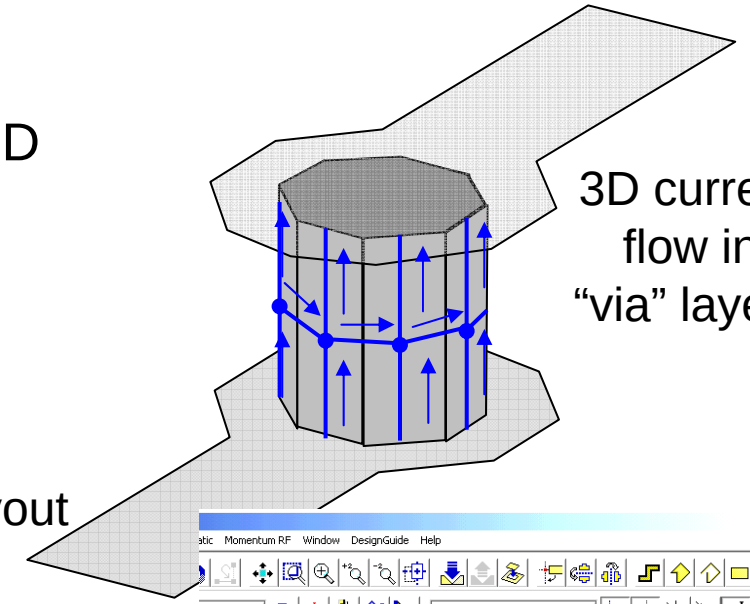
Upcoming improvements (2006A Update 1)

- Additional +30% raw Transient speed improvement
- New engine for robust handling of S-parameter data in the time domain:
  - Patent-pending new technology for built-in causality correction
  - Optional passivity correction

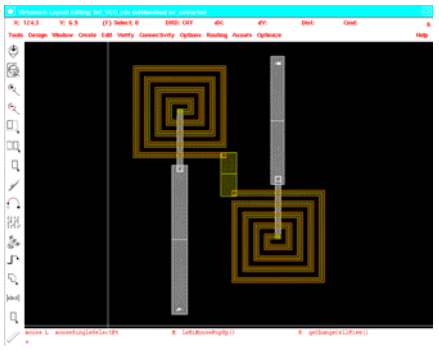
Momentum EM simulation

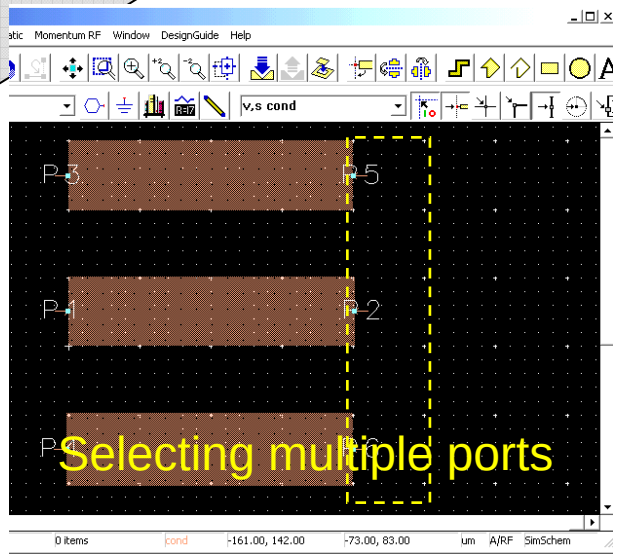
Continued enhancements for complex metallizations

- 64-bit solver handles larger problems
- Horizontal “via” currents allows truer, 3D current flow and hollow structures for accurate loss, reactance, and coupling
- UI improvements:
  - Working with ports
  - Ground reference pins optional on Layout “lookalike” components
- Improved Momentum compatibility with Assura for parasitic extraction (RFDE)



3D current flow in “via” layers





Selecting multiple ports

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Ptolemy Simulation - New Multirate Scheduler

Simulation Results (3GPP downlink source example)

	2005A	2006A	Performance Ratio (CLS / MS)
Memory	9 M	44 K	**207X**
Scheduling Time	298.81 sec	0.39 sec	**766X**
Total Simulation Time	360.38 sec	58.8 sec	**6X**

Benefits

- Increased capacity and robustness for some multi-rate simulations
- Efficient simulator with a smaller memory footprint for simulating more complex designs

64-bit Simulator Support in 2006

Breaks the 2 GB memory barrier to solve real-world problems

64-bit OS *(note 3)*	**ADS 2005A, RFDE 2005A** *(Momentum only)*	**ADS 2006A, RFDE 2006A** *(Momentum, Circuit, Ptolemy)*
Linux *64-bit AMD Opteron and Intel EM64T*	Red Hat WS 3.x *(AMD Opteron only)*	Red Hat WS 3.x, Red Hat WS 4.x, Novell SUSE Linux Enterprise Server 9.3
HP-UX	- - -	- - -
Solaris	8, 9, 10 *with 64-bit support turned on*	8, 9, 10 *with 64-bit support turned on*
Windows	- - -	Windows XP x64 (*ADS Momentum, Circuit only*)

1) Cadence and RFDE do not run on Windows. 2) More info at http://www.agilent.com/find/eesof-platforms
3) 64-bit Agilent simulator support varies when performed in conjunction with non-Agilent 32-bit device models and external co-simulations. May be subject to other restrictions, please ask your ADS specialist for details.

32-bit Operating System Support in 2006

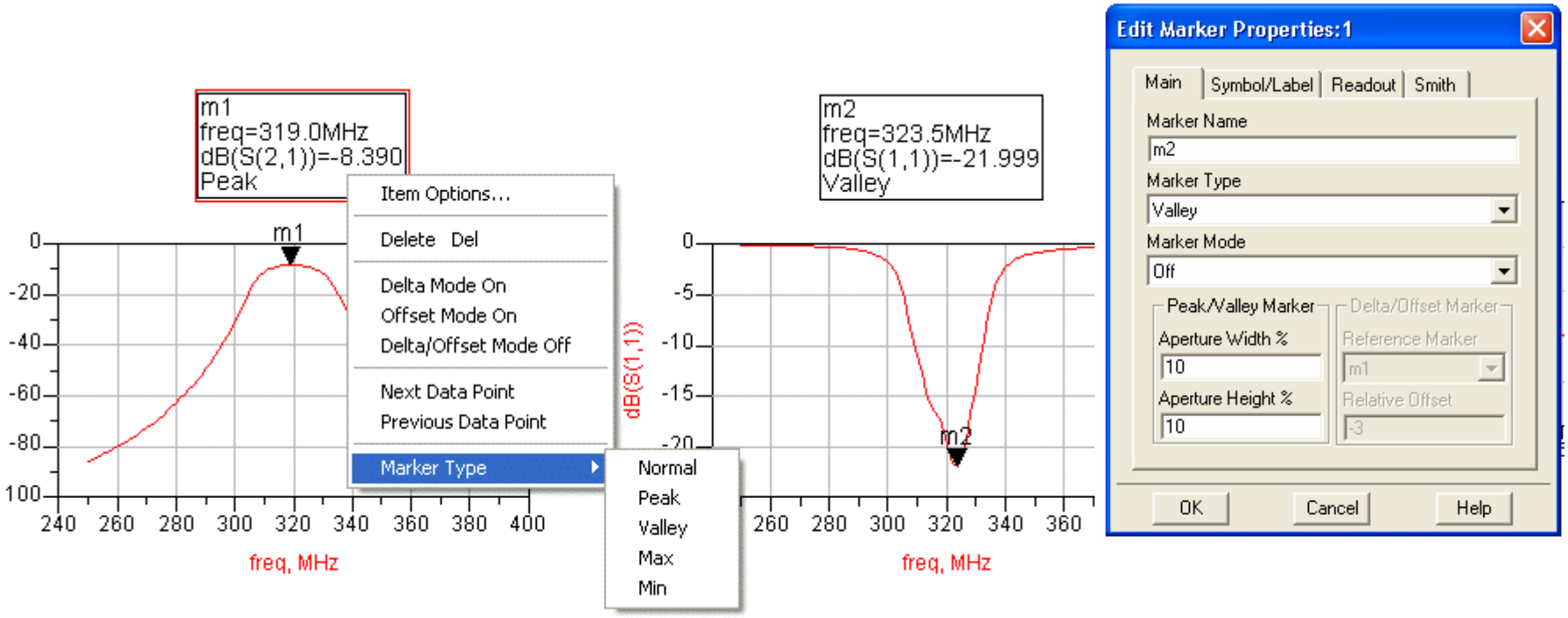
32-bit OS	ADS 2005A, RFDE 2005A	ADS 2006A, RFDE 2006A
Linux	Red Hat 7.2, 7.3, 8 Red Hat WS 2.1, Red Hat WS 3.x	Red Hat WS 3.x, Red Hat WS 4.x, Novell SUSE Linux Enterprise Server 9.3
HP-UX	11.0, 11i	11.0, 11.11 *(note 3)*
Solaris	8, 9, 10	8, 9, 10
Windows	Windows 2000 Pro, SP4 Windows XP Pro, SP2 *(note 1 - ADS only)*	Windows 2000 Pro, SP4 Windows XP Pro, SP2 *(note 1 - ADS only)*

1) Cadence and RFDE do not run on Windows. 2) More info at http://www.agilent.com/find/eesof-platforms
3) Agilent and many EDA vendors are not committing to support for HPUX workstations beyond 2006. See http://www.agilent.com/find/eesof-hpux-disco

Data Display –

New Marker Types: "Peak" and "Valley"

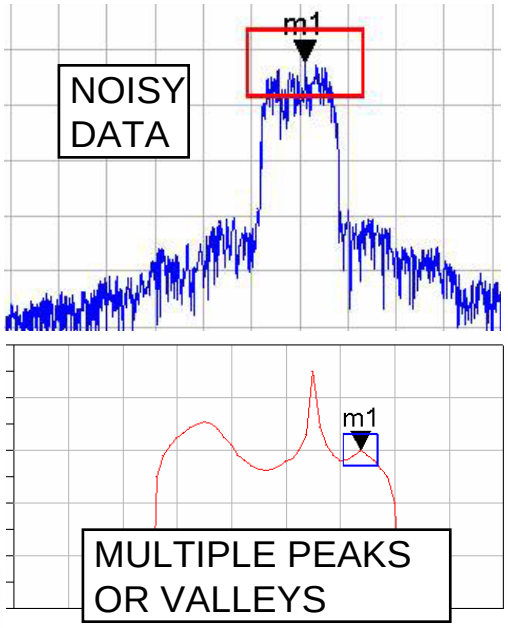
- Insert and drag like normal markers
- Snaps to peak/valley automatically, and can be used in delta-marker mode.

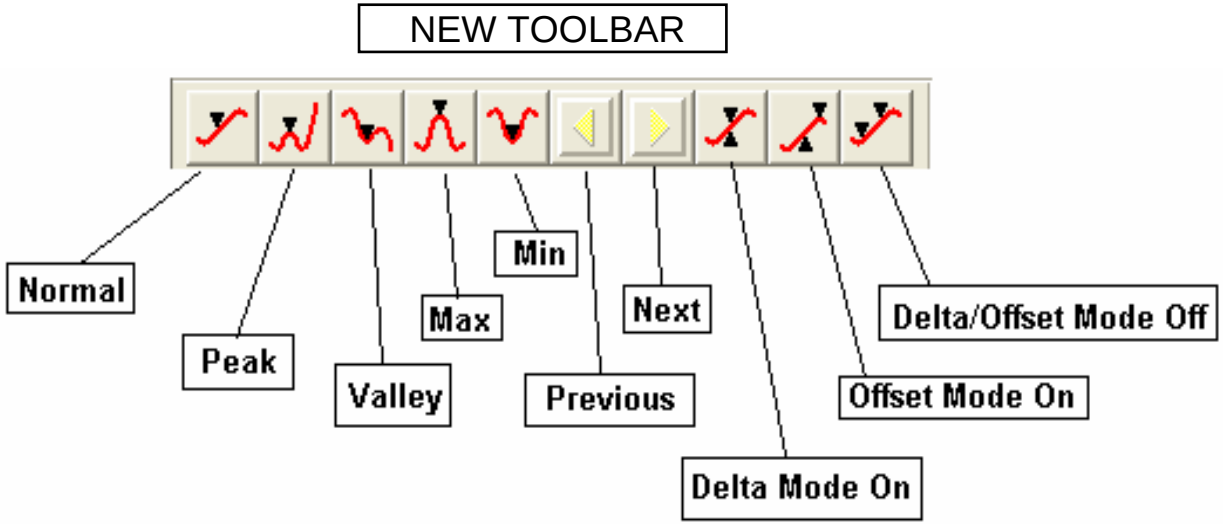


Data Display –

New Marker Types: "Peak" and "Valley"

- User-defined aperture adapts to noisy trace data and multiple peaks/valleys.
- Arrow keys, Pulldown, Popup and Toolbar buttons will advance the marker to the next/previous peak/valley.



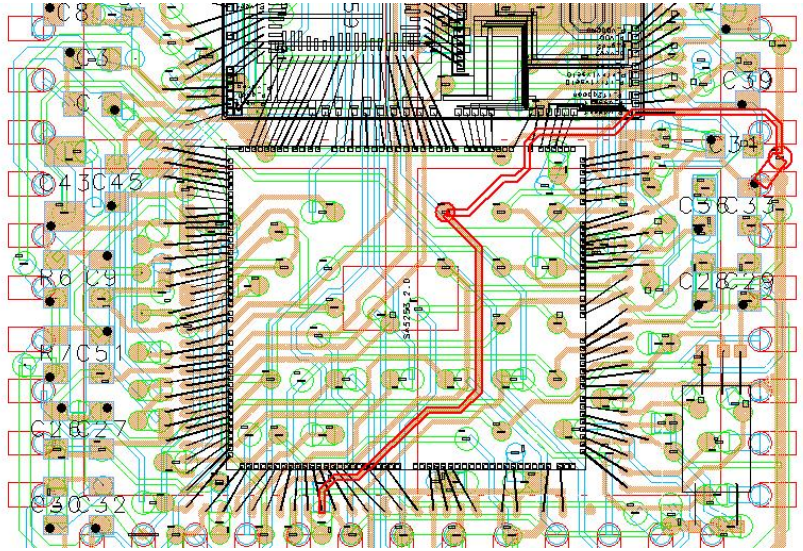


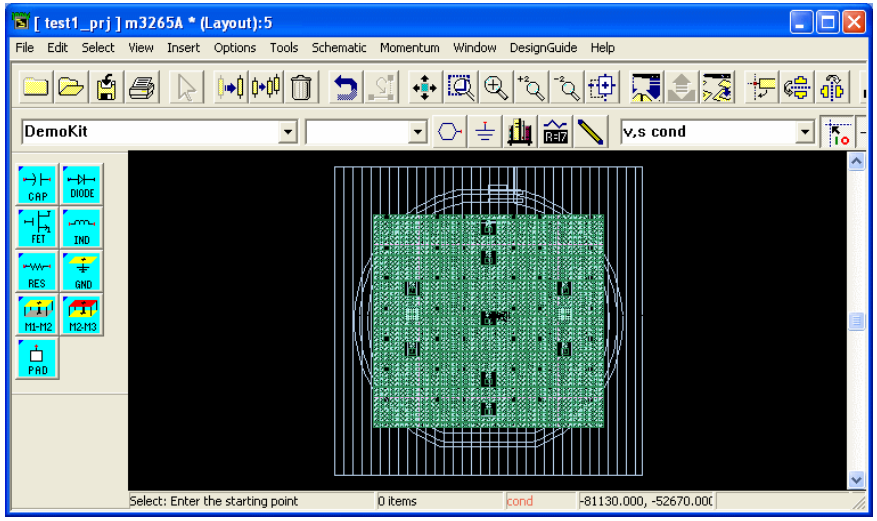
Layout – Performance gains with the new Physical Connectivity Engine (PCE)

- Significant performance gain for PCE for large designs.

- ADS 2005A could be slow when opening a large design for the first time
  → 2006A: almost no overhead for the connectivity engine

- 2005A User Interface to disable the connectivity engine was difficult
  → 2006A: easy “Preference” setting, but not necessary to disable





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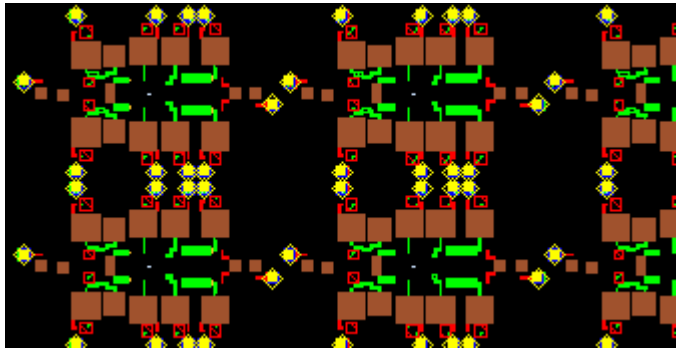
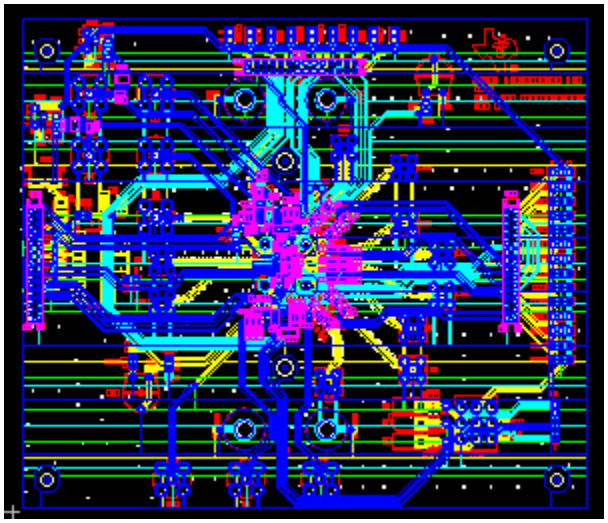
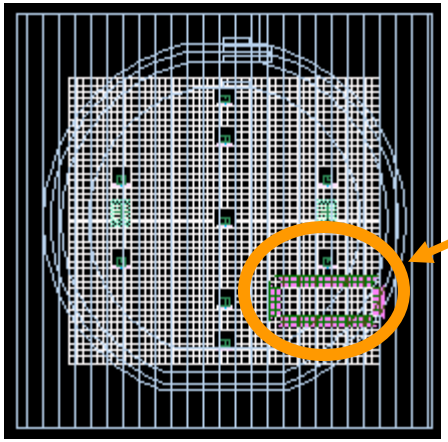
Layout – Performance gains with connectivity



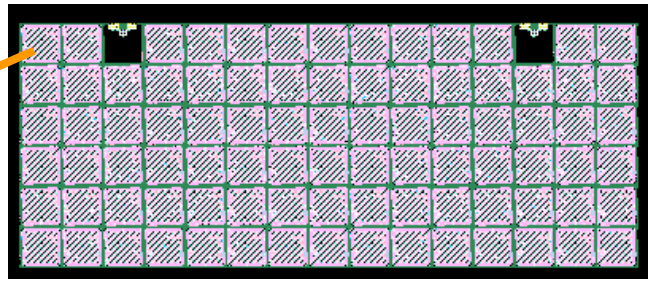
Array of 50x30 MMICs (1500 PA's)
2006A Load time: 20sec (18sec if PCE OFF)
2005A Load time: *Unable to load*



Flatten design (3500 shapes on 7 masks)
2006A Load time: 1.5sec (0.5sec if PCE OFF)
2005A Load time: 5sec



21 reticles of 15x6 PA array



Import GDSII file
2006A: 26sec (24sec if PCE OFF)
2005A: *Unable to import*

measured on a nc6000 1.4GHz Win2k

Layout – Performance gains with connectivity

- PCE passively maintains electrical connectivity in artwork without user intervention, wherever shapes touch
- PCE is a great trouble-shooting tool, highlighting:
  - DC paths, common nodes
  - Missed connections
  - Follows nodes across vias and layers
  - Dense layouts do not lend themselves to manual 3D connectivity inspection
- PCE is unique to ADS and in 2006A, PCE is fast.

Design	Connectivity off *(load time)*	Connectivity on, 2006A	Connectivity on, 2005A
1	< 1 sec	< 1sec, 52MB	2.3sec, 69MB
2	4 sec	5sec, 52MB	20sec, 216MB
3	30 sec	35sec, 67MB	load failed
4	5 sec	6sec, 55MB	16sec, 110MB
5	12 sec	12sec, 53MB	15sec, 69MB
6	22 sec	23sec, 54MB	>>120 sec, 300MB
7	72 sec	78sec, 130MB	1200sec, 630MB
8	9 sec	12sec, 13MB	17sec, 40MB

Table. The powerful connectivity mode of ADS Layout is fast, and prevents wiring errors in large boards, MMICs, and electromagnetic simulations.

There are performance improvements throughout Layout 2006A (e.g. - the “Chop” command, and more)

Improved Accessibility & Flow Integration in 2006

ADS & RFDE Platforms

Internet Download

Real-time Knowledge Search from ADS

Web-based SMT parts libraries

- Puts Agilent tools closer to design problems, deeper within your preferred design “flow”

- Real-time internet access puts IP at your fingertips

2006A Flow Integration – RFDE Platform

- Continued expansion of Spectre PDK compatibility
  - **Benefit: Direct foundry support for RFDE 2006A, with no intermediaries**.

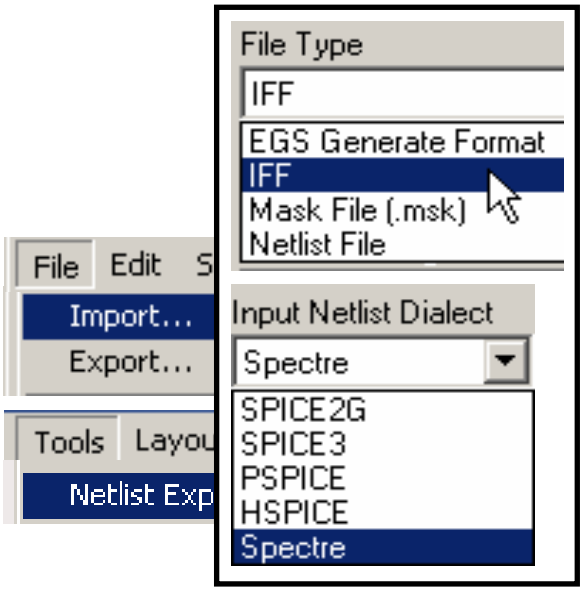
    The Top 10 RFIC silicon foundries worldwide (>95% of users) support RFDE 2006A directly. Agilent customers eliminate a critical dependence and risk on 3rd parties for their process design kits (PDK's)
  - **Result**: RFDE is now in use at the Top 10 RFIC semiconductor design companies, worldwide

- Assura compatibility for Momentum
  - S-parameter objects from Momentum handled more gracefully during Parasitic Extraction
- Continued investment in robustness of translators, PDK verification, and RFIP Encoder (encryption) for RFIC flows

2006A Flow Integration – ADS Platform

• 6 previously-licensed modules are now included free of charge with ADS 2006A

- **E8965, E8966, E8967, E8968 IFF translators**
  File-based translators that link to/from Mentor, Cadence, Eagleware
- **E8880 Spice Netlist import and export -**
  File-based netlist translators that link to new devices and processes
- **E8826 Ptolemy Matrix Models**
  Model set used for Matlab co-sim, data interleaving

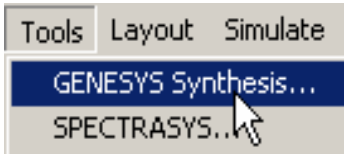


Free access to these connectivity modules when you upgrade to the ADS 2006A release

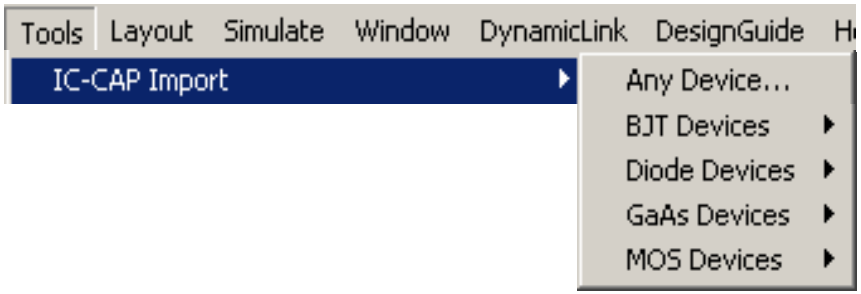
Additional ADS connectivity

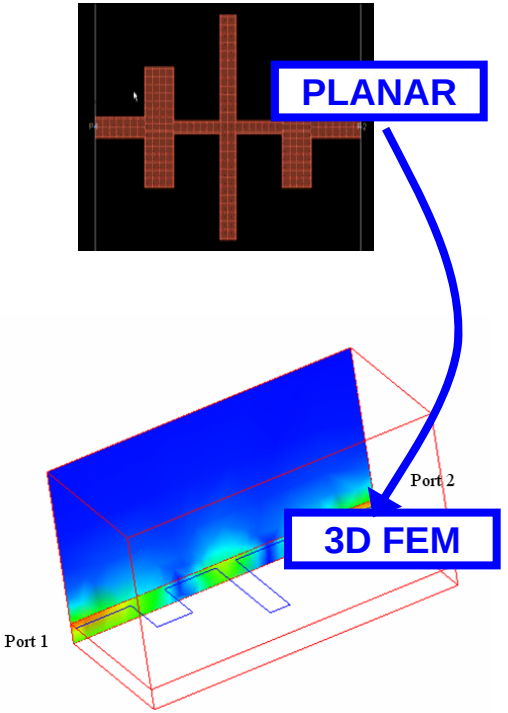
- Export Momentum (3D planar) projects to EMDS (3D finite-element)

- Live connectivity from Eagleware Genesys to ADS



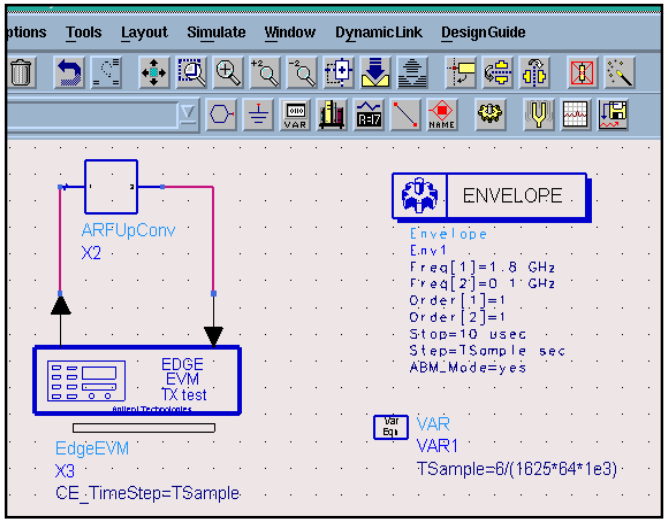
- ICCAP modeling data

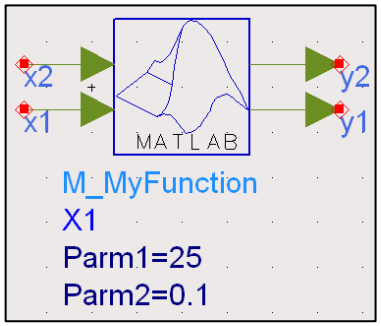




System Design connectivity

- Wireless Testbench (WTB) for Analog/RF
  - Create system testbenches in Ptolemy
  - Export them to ADS circuit environment
  - Analog designers embed the system object in the circuit schematic, but don't need to know how to use Ptolemy co-simulation
  - (Ptolemy co-sim requires Ptolemy license)





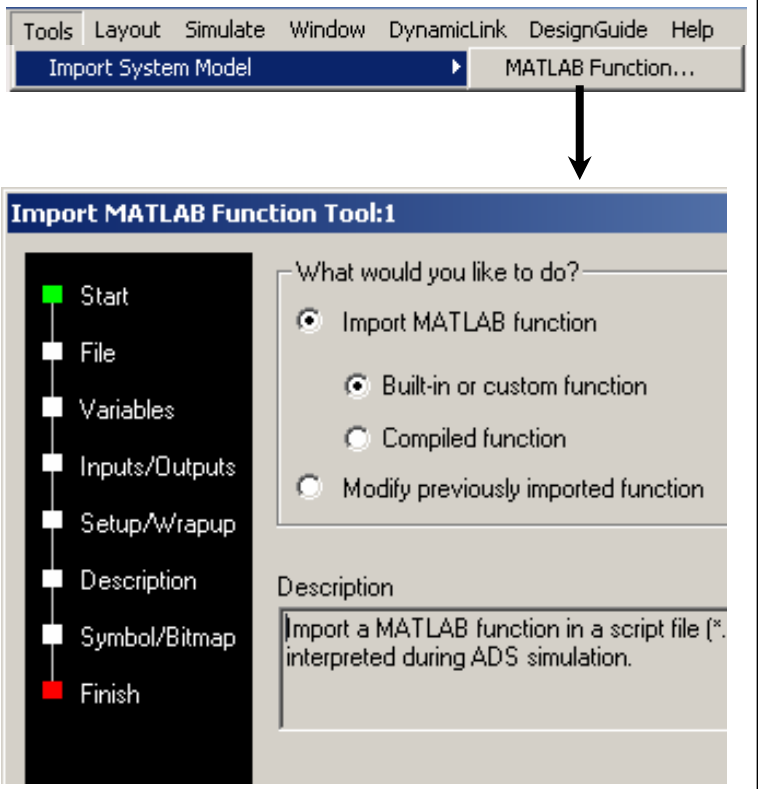
- Matlab Import wizard
  - preconfigures Matlab IP for easy co-sim with Ptolemy
- SystemC language-based support
  - Coming in ADS 2006A Update Release 1

MATLAB Import Wizard

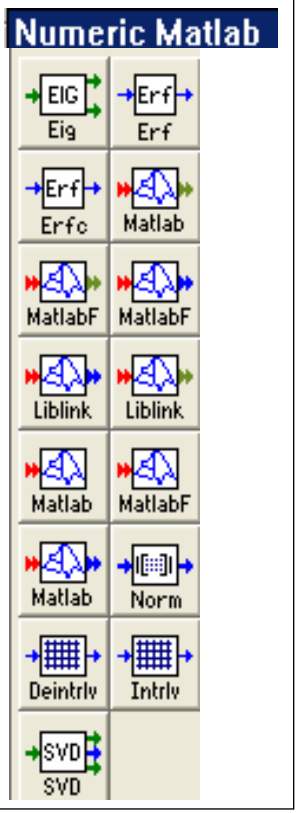
- Adds input/output ports
- Creates symbol, palettes, and bitmaps.
- Auto-generates ADS library components
- Automatically sets up Multi-rate operations
- Allows iterative update of generated MATLAB model
- Compiled MATLAB model support

Also: “Matrix Models” de-licensed in ADS 2006A

Import wizard



New palette



Agilent Technologies

Accessibility –
EEsof *Knowledge Center* is your One Source

Internet Downloads* (now in pilot testing)

- Full software releases for EMDS, ICCAP, RFDE and soon, ADS
- Patches, MSR's, "Update releases," Add-on products, and Early Access
- New examples and documentation, and more

New! Knowledge Search embedded within ADS

Log into *KC* today!

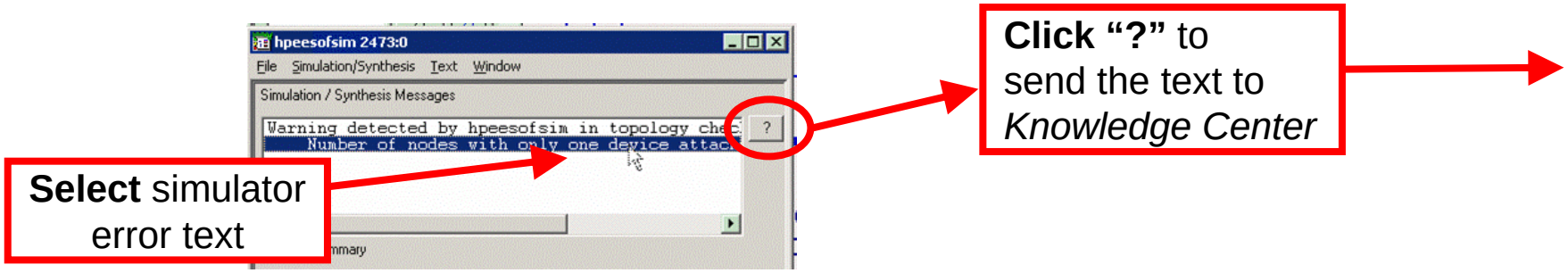
http://www.agilent.com/find/eesof-knowledgecenter

** Download performance and reliability can vary widely, due to factors outside Agilent control. May not be an alternative for all customers.*

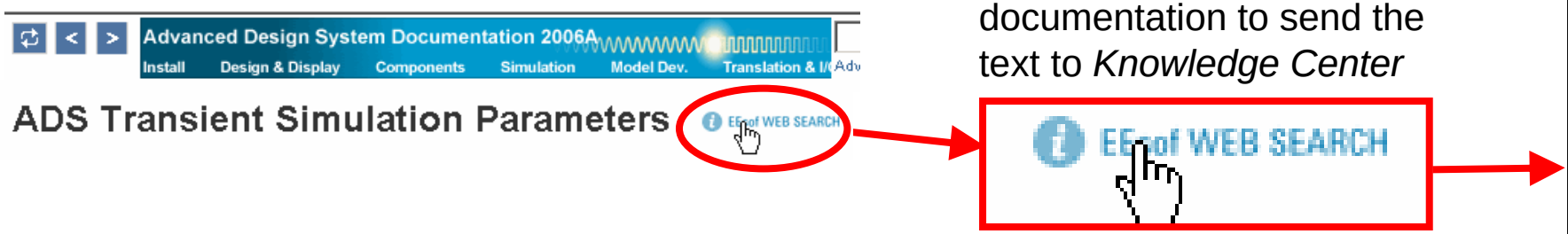
Embedded, real-time Knowledge Search

examples: A) from simulator, B) from documentation

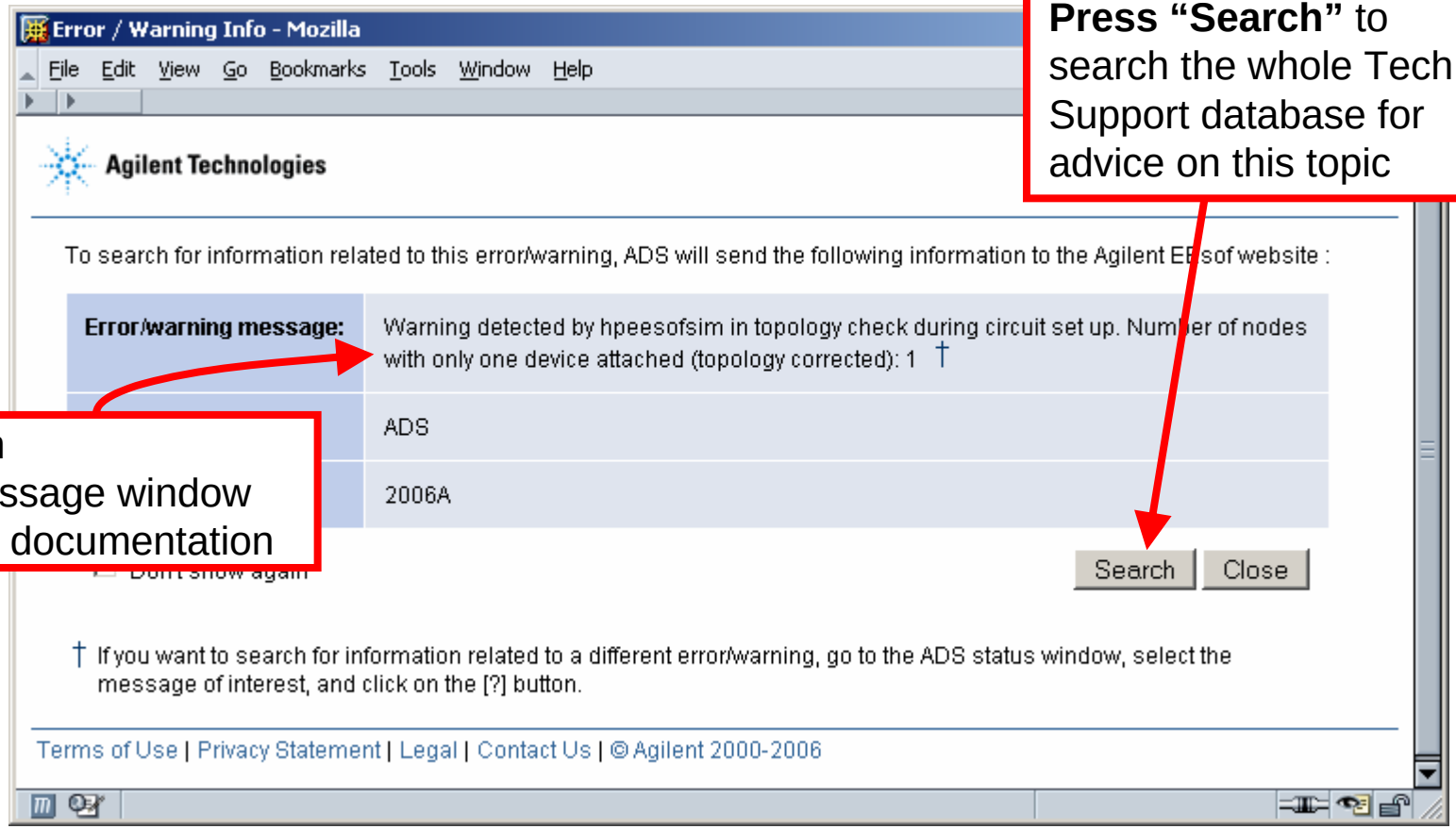
QUESTION:
What are my options for improving this simulation?



QUESTION:
Is there more information on this topic beyond the manuals?



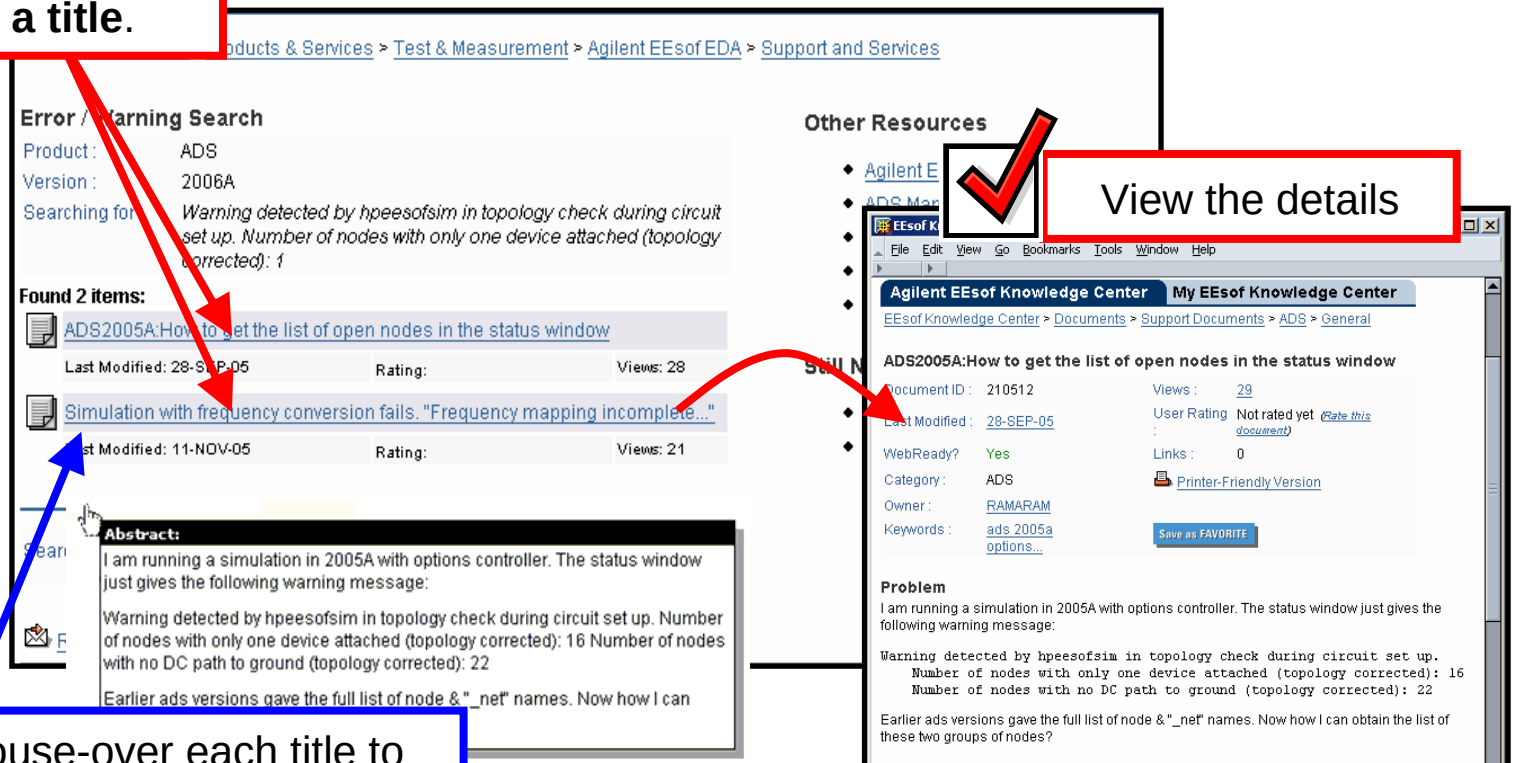
Embedded, real-time Knowledge Search



- *You <u>always</u> give permission before accessing the internet!*

Results of an embedded Knowledge Search

KC suggests two articles to view. **Click on a title**.



Mouse-over each title to see a quick preview, without logging into *KC*.

Benefits of embedded Knowledge Search

- Answer your own question 24 hours/day from the global Tech Support database
  - Practical explanations
  - Workarounds and advice
- Direct internet links from
  - Live ADS message window
  - Sub-headings in the ADS documentation
- Database expanding daily

Apply the worldwide experience of 1000's of other users to your problem, in seconds!

Customer Quote

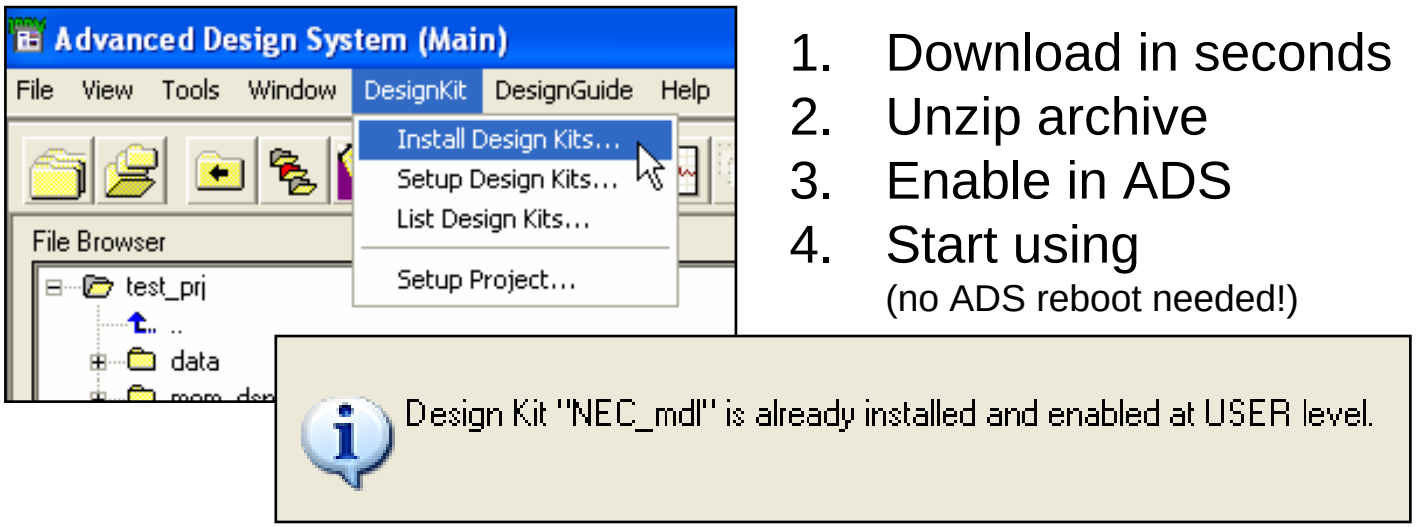
"Absolutely Yes.... I would definitely use this feature."

(at US defense contractor)

New SMT Design Kits install in a few seconds

- NEW! Over 30 vendors of SMT parts are now packaging ADS libraries in a standard “Design Kit” format for easy installation!

http*://eesof.tm.agilent.com/partners/vendor_libraries.html*

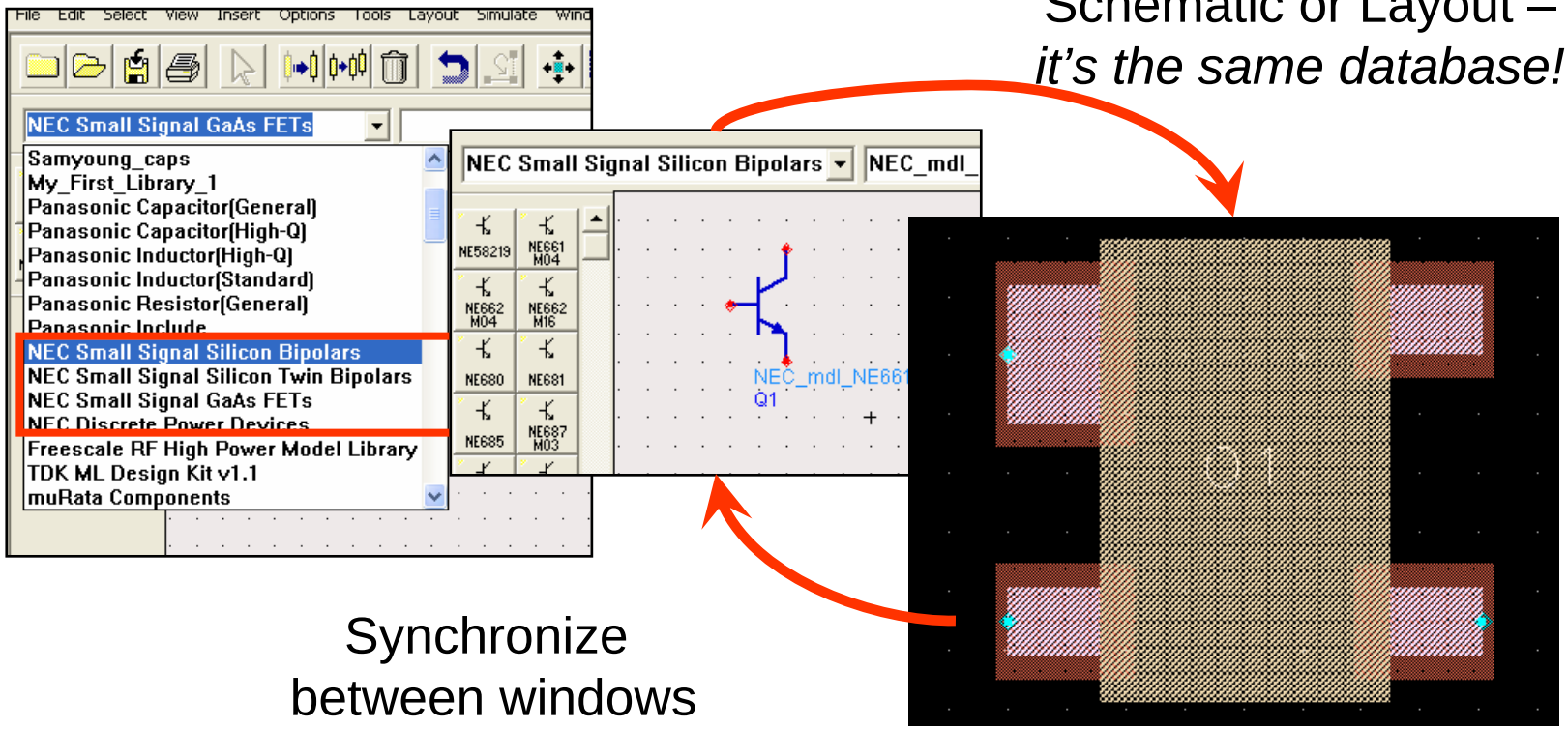


1. Download in seconds
2. Unzip archive
3. Enable in ADS
4. Start using
   (no ADS reboot needed!)

Fresh SMT Libraries in a few clicks!

Each vendor library enables a convenient Component Palette on the ADS schematic

Place SMT parts in either Schematic or Layout – *it's the same database!*



Synchronize between windows

Advancements in Quality & Usability in 2006

Quality & Usability in 2006

Customer Education in 2006

• Frees your creativity and makes the most of your design efforts

Advancements in Quality & Usability in 2006

Quality

- ~30% of 2006A traceable to a Quality Requirement (vastly improved)
  → *We're free to invest in new areas of long term value!*

- ~60% of 2006A specs are now traceable to Customer Requirements
  → *We listen to customers!*

Usability

- Addressed 250 customer-found defects and customer "annoyances"
- Dedicated Design Flow & Verification and Flow Marketing teams
  – Actively test the integrity of ADS for specific tasks, such as MMIC Design, during the software development process

Customer Education for 2006

- Over 20 days of classroom curriculum updated
  - ADS Quick Start
  - ADS Fundamentals
  - ADS Advanced Circuit
  - ADS Layout
  - Momentum for ADS Users
  - ADS Communication Systems
  - ADS Signal Processing
  - ADS Signal Integrity
  - RF Design Environment
  - Momentum for RFDE Users
- 2 Electronic web-based courses updated
  - ADS Fundamentals e-Learning course
  - ADS Layout e-Learning course

The 2006 releases of ADS help High-Frequency Designers to

"*Start Closer to the Finish Line*"