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A High-Performance 14.4 to 19.7 GHz Power Detector Fabricated with Flip-Chip Technology

Abstract

A rugged flip-chip technology with potential for low cost at high manufacturing volume was employed to fabricate a power detector using mixed device technologies. The circuit consists of one discrete GaAs pHEMT chip and one GaAs dual-Schottky-diode chip flip-attached to a 3.5 mm x 2.1 mm substrate containing only passive circuitry. The power detector offers two different modes of operation to enable compensation for drift of the detector diode response over temperature. In the first mode, a circuit was demonstrated to provide better than ±1.05 dB flatness over the 14.4 to 19.7 GHz frequency range when operated over the –4.5 to +16.5 dBm input power range at room temperature. In the second mode, the flatness over this frequency range was better than ±0.8 dB when operated in the –7.5 to +16.5 dBm input power range at room temperature. The minimum return loss was better than 30 dB, and the maximum insertion loss was 0.21 dB.

Summary

As part of an effort to reduce costs and simplify millimeter-wave circuitry for mass production, an MLMS™ (MultiLithic MicroSystem™) technology has been applied to a power detector that had previously been implemented in chip-and-wire technology with multiple discrete components. In MLMS™ technology small semiconductor dice containing the active elements are flip-attached by way of an automated assembly process to an inexpensive substrate that contains all of the passive elements of the circuit or subsystem. The attachment is achieved via thermocompression welding of pads on the semiconductor dice to 30-micron-diameter gold bumps on the substrate—the same metallurgy as in wire bonding. These assemblies withstand repeated cycling between liquid nitrogen and a 300 °C hot plate and repeated cycling between freezing and boiling while under water. They have been tested under mechanical shock at 3000 Gs, and, based on measured die pull forces, are expected to withstand 100,000 Gs.

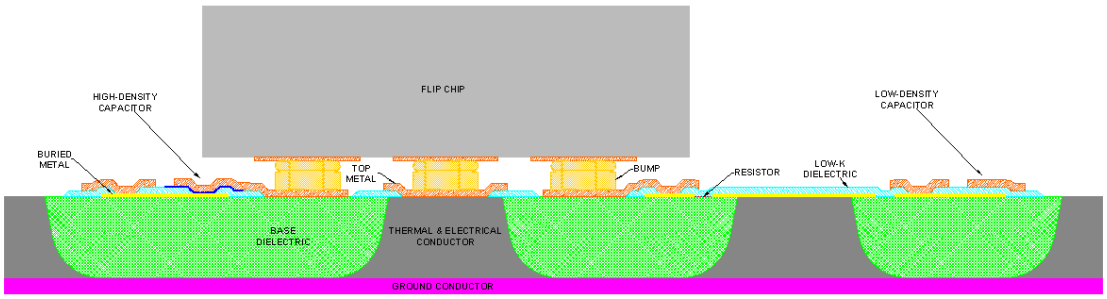

Figure 1: Conceptual cross-section of a semiconductor die flip-attached to a passive substrate

The MLMS™ substrate, a cross-section of which is shown conceptually in Figure 1, has built into it high-thermal-conductivity pedestals that are precisely shaped to thermally ground a bump while maintaining electrical isolation to other bumps spaced as little as 65 microns away center-to-center. Consequently, each flip-attached die can be less than 0.3 mm by 0.3 mm square in size and can have a thermal resistance equal to that of a 100-micron-thick die eutectically attached by its back side to a heat sink.

The MLMS™ power detector chip, shown in Figure 2, consists of a 3.5 mm by 2.1 mm substrate with one pHEMT (pseudomorphic high-electron-mobility transistor) die and one dual-Schottky-diode die attached to it as part of the functional circuit. One additional die of each type was also attached for quality control purposes. The dual-Schottky-diode die was custom fabricated with a distinct high-cutoff-frequency process. Figure 3 shows the block diagram. The circuit comprises a high-directivity coupler with a broadband termination, two fixed-value attenuators, an SPST (single-pole, single-throw) switch, and a diode pair with associated biasing and matching network elements. DC biases to the detector and

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reference diodes are fed by 70 µA constant-current sources, and a control voltage may be alternated between –1.6 V and 0.0 V to open and close, respectively, the pHEMT resistive switch. The bias lines are individually filtered on the passive substrate.

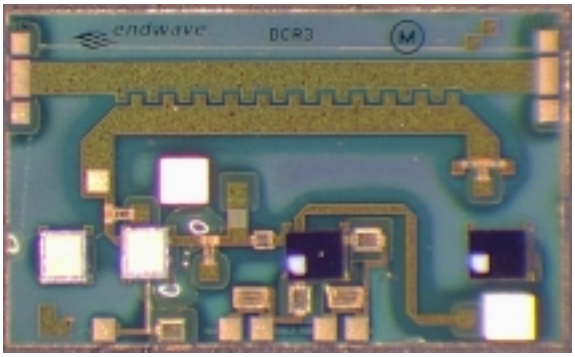


Figure 2: Assembled power detector chip

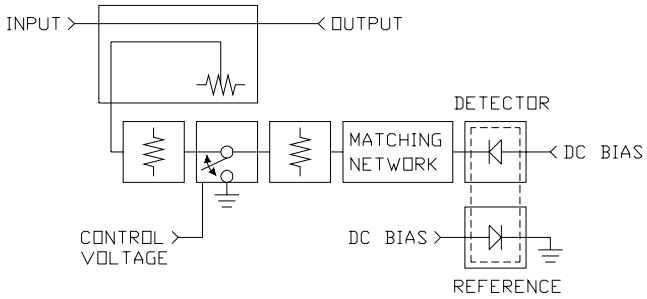
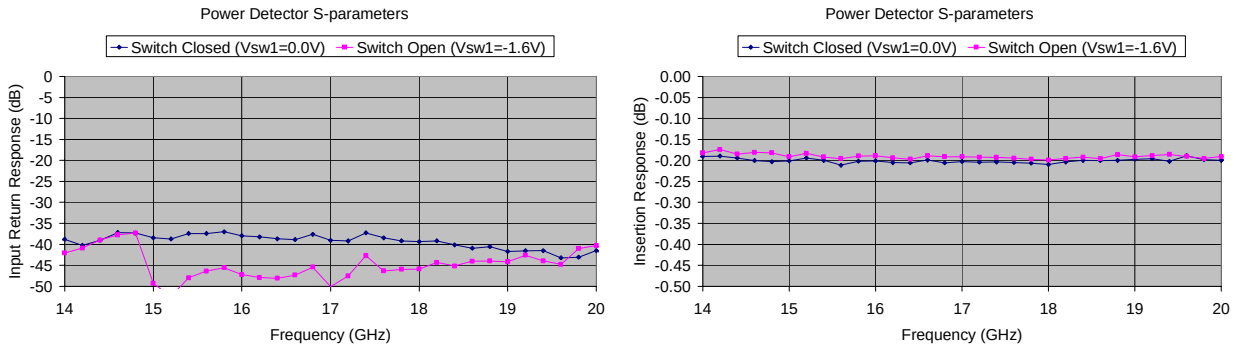


Figure 3: Block diagram of the power detector

This circuit enables two modes of operation. In the first mode both diodes are equally biased, and the switch is biased to be in the open state; the detector diode DC voltage is subtracted from the reference diode voltage to determine the RF input power level. This mode of operation will be referred to as the "reference" mode. In the second mode only the detector diode is biased, and the SPST switch (referred to as a "chopper") is toggled between the open and closed states so the detector diode is alternately exposed to and isolated from, respectively, the available coupled RF power. The difference between the detector diode voltage during the closed-switch state and the detector diode voltage during the open-switch state is taken to determine the RF input power level. This mode of operation will be referred to as the "chopper" mode.

Small-signal S-parameter measurements of a power detector sample were measured on a probe station using a TRL calibration, and the RF performance is shown in Figure 4. The minimum input return loss is better than 30 dB and the maximum insertion loss is better than 0.21 dB over the 14 to 20 GHz output frequency range.



(a) (b)

Figure 4: Measured (a) return responses and (b) insertion responses versus switch control voltage

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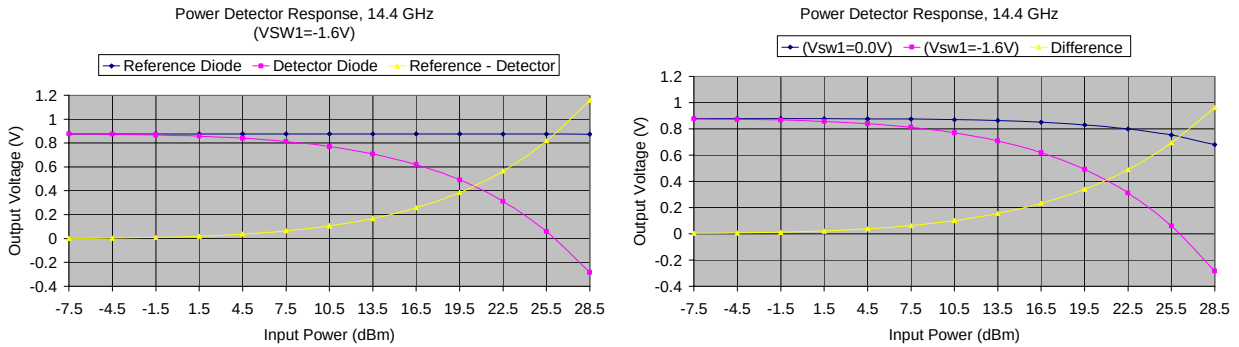
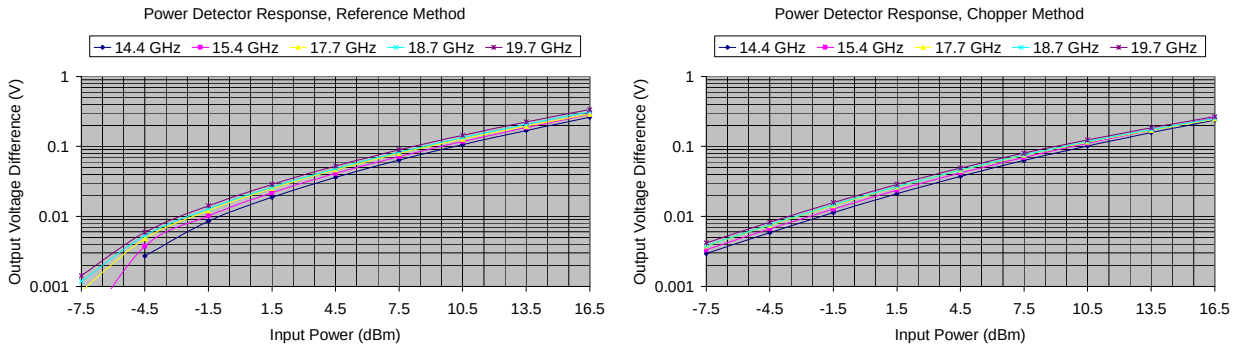


(a) (b)

Figure 5: Measured responses of the power detector at 14.4 GHz when operated (a) in the "reference" mode with the switch held open, and (b) in the "chopper" mode with the switch toggled between the open and closed states.

The differential voltages for each frequency are graphed in Figure 6 for each of the power detector's two modes of operation. From these responses it is evident that the detector has more dynamic range and better flatness over frequency when operated in the "chopper" mode than when operated in the "reference" mode. The improved dynamic range results from the use of a single diode for both detection and reference. In the "reference" mode, even though the reference and detector diodes are part of the same die, a slight mismatch can affect the results. The flatness of the "reference" detector may be improved over a portion of the input power range through the addition of a DC offset to the difference between the diode voltages.



(a) (b)

Figure 6: Measured responses of the power detector over frequency when operated (a) in the "reference" mode with the switch held open, and (b) in the "chopper" mode with the switch toggled between the open and closed states.

A chip-and-wire technology implementation of the "chopper" design uses 7 discrete chips and 10 interconnect bonds. To implement the MLMS™ circuit, only a substrate with two flip-attached devices and 5 interconnect bonds are required. In addition, the MLMS™ circuit is expected to achieve more repeatable performance than the chip-and-wire solution due to fewer potential variations in manufacturing processes.

Conclusion

A technology that allows flip attachment of small devices of various types to a high-precision passive integrated circuit substrate has been utilized to simplify the assembly of a power detector. A design requiring assembly of multiple discrete chips via chip-and-wire technology can be replaced by one employing a single rugged multilithic integrated circuit offering the potential of improved performance and lower overall cost.