Managing Phase Noise in Microwave Chains

Marjan Grman

Iskra Sistemi, d.d., Stegne 21, Ljubljana, Slovenia SI-1000,
e-mail: marjan.grman@iskrasistemi.si

Abstract. This work encompases a set of phase noise and some other rules for microwave oscillator design in microwave receiving and transmitting chains intended for SDR radio systems. Engineering shown in this work, comes from error vector magnitude achievable in a system. A 10 dB difference between demanded EVM and CINR is a reserve needed for compensating of various errors, wich are inevitable caused by the elements in the frequency conversion chain. Using this design process, post-layout simulations show a phase noise of -110 dBc/Hz at the offset of 100 kHz.

Keywords: phase noise, SDR, EVM, reserve, conversion

1 Introduction

Noise in oscillators is an old and new issue. It yet sometimes confuses even professional engineers, because oscillation itself is essentially an autonomous phenomenon.
This paper is formatted to discuss the complete design of the frequency conversion chain using the end user approach (or application aspect) presented, viz. from the design specifications, concept designs, subsystems, simulation results and eventually conclusion.
Software defined radio (SDR) is now popular in wireless comunications. The technology is an enabler for many new variable capacity applications and cognitive radio. [21] This work tries to enlighten one, many times overlooked, but very important aspect in the designing of the SDR radio system. A major challenge for software defined radio is to equal the efficiencies of pure hardware solutions, while providing the flexibility and inteligence that only software can provide.
Radio system software developer will want to be shielded from all hardware (HW) developmental changes. On customer demand, he will only want to upgrade the multilevel digital modulation and bandwidth. Maybe even a digital protocol of radio-to-radio communication. What this will pull behind, one can only imagine. But some things are certain. Protocol can demand more memory and CPU resources. Higher speeds and higher level digital modulations will demand higher frequency amplitude dynamic and phase noise conditions in the rx/tx frequency conversion chains (HW) alone. [17] In good systems, with enough amplitude dynamic, these low noise conditions can only come from local oscillators. Power supplies and active lowpass filter must be made low noise. Electromagnetic shielding must be reasonable enough.

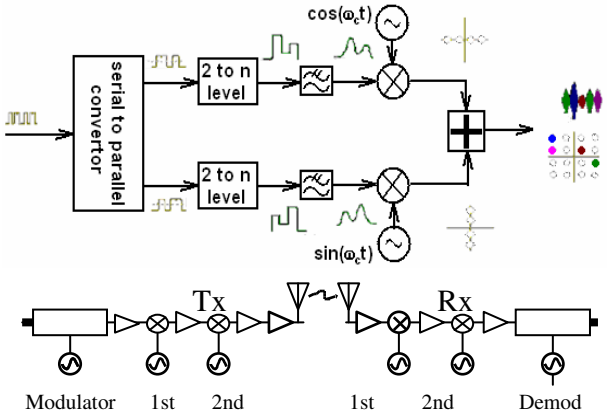

Figure 1. (above) Typical multilevel digital modulator that requires low PN oscillators. Parameter n is set to 4 levels, so 16 QAM could be generated. [22] (below) Typical block schematic of radio link connection employing digital multilevel modulation, relevant for understanding of PN influences.

It was also noted, that so called golden units, which were sometimes used for certification purposes, because they were not dribbling errors all the time, were not much more than the units whose phase noise was much lower than with the other units. [1]

2 Phase noise (PN) according to modulation

Phase noise and timing jitter are both measures of uncertainty at the output of an oscillator.

Phase noise defines the frequency domain uncertainty of an oscillator. If the output of an oscillator is given as $V(t) = V_0 \cos[\omega_0 t + \phi(t)]$, then $\phi(t)$ is defined as the phase noise. This expression of noise is useful for analog designers in situations such as RF design when the spectral content is of importance in determining the interference of out of band signals. In case of small noise sources (a valid assumption in any usable system), a narrowband modulation approximation can be used to express the oscillator output as:

$$\begin{aligned} V(t) &= V_0 \cos[\omega_0 t + \phi(t)] \\ &= V_0[\cos(\omega_0 t) \cos[\phi(t)] - \sin(\omega_0 t) \sin[\phi(t)]] \\ &= V_0[\cos(\omega_0 t) - \sin(\omega_0 t)\phi(t)] \end{aligned} \quad (1)$$

This shows, that phase noise will be mixed with the carrier to produce sidebands around the carrier, giving a direct connection between phase noise and the spectral output of the oscillator. The noise spectral power density of an oscillator is given in decibels below the carrier per Hertz (dBc/Hz) and is defined as: [18]

$$\begin{aligned} \pounds_{total}\{\Delta\omega\} &= 10\log_{10}\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right] = \\ &= 10\log_{10}[S_\phi(f)] \end{aligned} \quad (2)$$

We usually observe the asymptotic behavior of phase noise $\pounds(f)$ measured at an offset frequency f from the carrier and assert that:

$$\pounds(f) = \frac{a}{f^2} = \frac{1}{\pi}\frac{\pi f_{osc}^2 c}{f^2} \quad (3)$$

where a is some constant. But this implies that phase noise goes to infinity at $f = 0$. This is obviously wrong, as it implies that there is infinite noise power at $f = 0$. It is also a simetrical function to the vertical axis. Therefore, half of it is enough for correct mathematical description of phase noise (PN) designated as sigle side band (SSB) in this case.

For very noisy oscillators, it could also suggest that $\pounds(f) > 0$ dBc/Hz at small enough offsets. But phase noise has been shown to have a Lorentzian spectrum:

$$\pounds(f) = \frac{1}{\pi}\frac{\pi f_{osc}^2 c}{\left(f_{osc}^2 c\right)^2 + f^2} \quad (4)$$

where c is a scalar constant that describes the phase noise of the oscillator (in the absence of $1/f$ noise and ignoring any noise floor). This choice of expressing the characteristic constant as $\pi c f_{osc}^2$ will become clear when the constant c is reused in the equations for jitter. The Lorentzian spectrum nicely avoids any singularities at $f = 0$ while maintaining the same asymptotic behavior. It also has the property that the total power in $\pounds(f)$ from minus infinity to plus infinity is 1. This means that phase noise does not change the total power of the oscillator, it merely broadens its spectral peak. If we borrow some terminology from laser technology (lasers are just optical oscillators), we can talk about the spectral line width of an oscillator (also half power width, full width at half maximum, or –3 dB width f_{HW}):

$$\pounds(f) = 2 f_{HW} = 2\pi f_{osc}^2 c \quad (5)$$

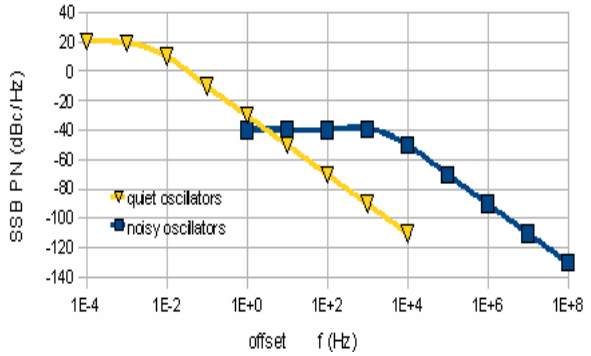

Figure 2. Typical SSB phase noise characteristic for quiet and noisy oscillators. [8]

For quiet oscillators (Figure 2), the phase noise at offset frequencies greater than 1 Hz will always be less than 0 dBc/Hz, avoiding the embarrassing question of what a phase noise greater than 0 dBc/Hz means (Figure 2). At some very small frequency less than 1 Hz, the phase noise will be greater than 0 dBc/Hz, but only within a bandwidth of a fraction of a Hertz. This is what we should expect, to see something representing the carrier signal itself at $f = 0$, which in the absence of noise would have a spectrum of $\delta(f)$. Figure 2 shows the phase noise for $\pi c f_{osc}^2 = \pi \times 10^{-3}$. We can see

phase noise greater than 0 dBc/Hz, but only at an offset frequency of less than 0.03 Hz. The total power integrated over a 1 Hz bandwidth is still unity. [8]
Then there is Colored Noise Sources, jitter, Absolute Jitter, cycle-to-cycle jitter, which are all different statistical method tools of describing phase noise and different looks of it. I am using RMS noise given in degrees to describe effective noisyness of either the oscillator or the complete chain in usable bandwidth of the baseband signal and a little more - just in case.
Figure 3 gives results for different multilevel digital modulation schemes. It is given in correlation to carrier phase. This is out of the scope for this article and I am not going into details of it. But very quiet oscillators are the topic in which every microwave radio engineer should be very much interested.
High phase noise is actually good for the company. That is, if radio engineers can live with. This is also the case for the VCO manufacturers, who have less concern of VCO refusing to start at power up.

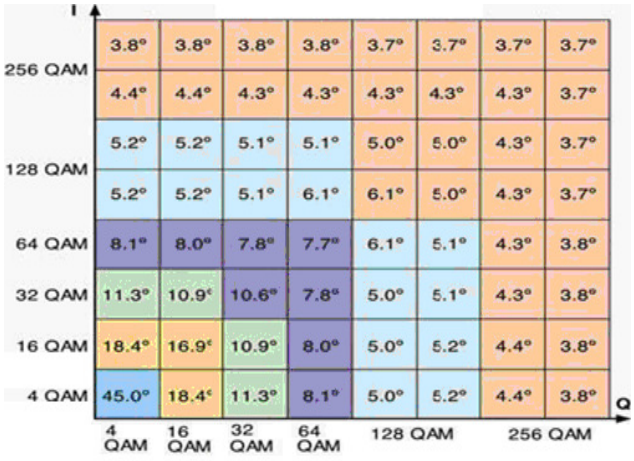

Figure 3. The maximum angular error between the center of the symbol and the symbol boundary for each symbol point and various digital QAM modulation methods. [3].

The maximum tolerable carrier phase anomaly is only 3.7 degrees for a 256 QAM signal (before a symbol error or syndrome is created). This is a goal for SDR chains. From that we can see, how little there is a margin for error in case of 256 QAM multilevel digital modulation. [3] Less complex constellations, with fewer points, are less sensitive to phase anomalies in carrier.

3 Frequency Conversion Chains

In radio and signal processing, heterodyning is not a new process. It is a generation of new frequencies by mixing of two oscillating waveforms. It is useful for modulation and demodulation of signals in digital domain. On the other hand, it is a tool for placing information of interest into a frequency range more conveniant for transmission over larger distances. [20]
Actual frequency conversion chain that was looked into in this case, is receiving chain. It converts receiving frequency towards a more managable value for the A/D convertor. These days, they are a common occurance in the software defined radios. In Tx chains it is a vice versa process that begins with a D/A coverter. But even the receiving chain gives good enough view into the mixing process of a noise component.
Operation may be accomplished with a vacuum tube, transistor, or other nonlinear device. [10] The simplest frequency conversion device is a diode. It is essentially a nonlinear element, that allows mixing of several signals of different frequencies and amplitudes. The one such mixing element (or mixer) seems to be enough for every down/up conversion in the world. But in frequency conversion chains, multiple mixing stages are almost always implemented. Why is it almost always so? Is it because, mixer manufacturing companies would like to sell some more mixers? No. This is because a nonlinear element must not be driven into a saturation with local oscillator so much, that it would be destroyed from so much dissipation. Input power needed to achieve a required output power at the required frequency would be too great, due to the large mixing losses. By that, I do not have in mind a mixer with an inbuilt amplifier.
At the same time the harmonic content would be so rich, that it would fall into the user band and spoil the information bearing signal actually usefull to the operator of microwave radio link.

3.1 Balanced mixers

Different kinds of mixers can be built from diodes. Only single diode is not so good as a mixer, because it cannot suppress local oscillator signal. Balanced mixers can do it much more effectively. This is one aspect that was mostly ignored in this case, as PN was measured on different carriers at the output of the down-converters.

Therefore frequency conversion chains are required for frequency conversion, which must be done gradually (Figure 4). In that case, theirs behaviour is only based on the simple mathematics of multiplying various sinusoid signals. Mixing two frequencies creates two new frequencies, according to the properties of the sine function. One is created at the sum of the two frequencies mixed, and the other at their difference [10]. In that case we say, that mixers operate in a "linear" mode. These multiplications can result in a whole range of summed and subtracted input frequencies and theirs multiples. The number of the resulting frequencies is direct result of mixer "nonlinearities" and various signal levels.

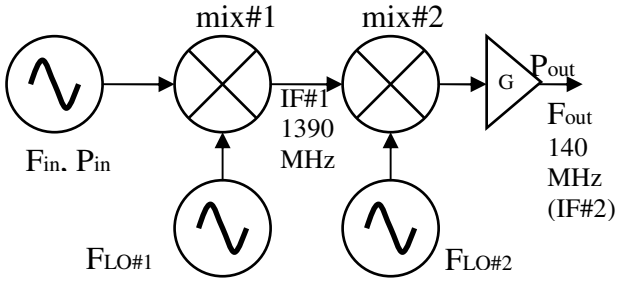

Figure 4. Principle block schematic of a microwave frequency conversion chain and local oscillators

The chain should convert frequency only and must therefore not change an amplitude content in any way. It may even have to amplify it. Amplitude decrease due to conversion losses can be easily corrected with amplifiers and then the attenuators.

To change a spectrum content, we must use filters or any other tuned circuitry that is available. And it is not necessary that it can be done with the chosen set of freqencies and physically available filters. This is valid for receiving (Rx), as well as for transmitting (Tx) chains alike. Group delay issues must also be taken into the account in actual signal conveying circuits. That holds true even more so, if radio chips (which can include complete system on a single chip) cannot compensate for it.

The aim of this work was to check PN in Rx/Tx chain with new components from Hittite. I also tried to take the Earth environment issue into consideration by choosing the all ROHS test components.

A theory behind this frequency conversion operation for a chain is that, if I multiply frequency, I loose PN performance (PN increases) and v.v. The theoretical factor in both cases is given in dB by (10). A 3 dB of PN performance would also be lost, when two equally noisy signals are summed. This is the same situation, as if noise power would be added to them. I assume my PN is white noise at all times and points anywhere in the frequency conversion chain, so that it can be liberally added power wise. The theoretical factor is most usefull for choosing a frequency of the local oscillators $F_{LO\#1}$ and $F_{LO\#2}$.

I refer to a single frequency oscillator output as a signal as it is noise modulated and therefore its spectrum is a little bit widened. It is not a single component as may be expected, but can be sometimes approximated to one alone.

Mixing in a frequency conversion Rx/Tx chain of a heterodyning type is a straightforward process. This means that correction of PN is not possible after the mixing, which is a frequency conversion process. This is so in Rx downconverting as well as in Tx upconverting chains. This is all in accordance with the stepped frequency conversion theory described earlier in this article.

This way, frequency converting chains can be described as downconverting, if $F_{out} < F_{in}$. First oscillator frequency $F_{LO\#1}$ and second oscillator frequency $F_{LO\#2}$ must match these reqirements. In our case is $F_{LO\#1} > F_{LO\#2}$. P_{out} is in this case an output power of interfrequency signal and F_{out} is targeted output (inter)frequency 140 MHz of the chain.

So the only way to keep a PN at the end of a chain in check, is to keep all of the input sources noise free as much as it is technically possible. This also means encasing certain portions of the circuit in electromagnetic barriers (physical enclosures) or at least

keeping them separated well away from potential powerfull noise sources.

3.2 Power supply influences on PN

Phase noise also gets influenced by pulling/pushing in VCOs via its power supplies. They tend to broaden RF output signal spectrum of VCOs. HMC510LP5E has 20 MHz/V pushing factor @ +5 V power supply, which must be taken into consideration. It means that VCOs frequency is also dependant from power supply voltage. The same holds true for the other VCO used, the VM585ME58-LF. It has 4 MHz/V pushing factor @ +10 V power supply, but at the lower frequency. Noise in power supply frequency modulates output signal and broadens it.
Countermeasures should be made as simple as possible - to decrease the noise from the power supplies. Power supply should be very well designed by carefull choosing of its components.
Power supply noise is of a special concern. Designer can do away with this issue, if power supply designed, is isolated enough from all possible noise sources as much as it is technically possible.
Power supply stabilization was done in two stages. The stirdy first stage provides more coarse voltage limitation for very sensitive secondary voltage stabilization circuits. The second stage actually provides maximally fine noise reduction in power supply for very sensitive and critical parts of the chain, like oscillators, mixers and amplifiers.
Noise gets to an output signal too, mostly from pushing of VCO and some via a cross-line coupling in a circuit. So, using as quiet a power supplies as possible in ultra low noise oscillators of this kind, is a must! Particular care was taken in finding those ultra low noise power supply chips from Linear Technology company. Only all of this care to noise details in a circuit would ensure full exploatation of a potentially very low noise VCOs from Hittite and Z-Comm. Power supply chips employed in particular oscillators are:
- LT1965EMS8 for low noise power supply of PLL filter amplifier,
- LT3878MR-ADJ is used as a + 5 V power supply for low noise currrents up to 0.5 A, mainly for HMC510LP5E VCO and charge pump operation of HMC700LP4E synthesizer chip,
- LT5900-3.3V chip for + 3.3 V power supply. It is especially sensitive to the input overvoltage condition. In this utmost care is advised at powering up this chip (overvoltage is a special concern), because not only this chip goes when it happens.
Low dropout regulators (LDO) are used in final stages of power supply regulation. These are meant mostly for battery operated applications, to conserve energy, which is always good these days. This prolongs operational time. But in this case, they were used as a very fine voltage stabilizers. For all that, it is pretty much irelevant what their power supply is. Input voltages for them are always much more stable than the batteries, but more noisy too! This ensures even better stabilization, but the noise issue in all of that is critical. That is even more important, as they can only stabilize effectively an output voltage, that is lower than the input. The lowest differential voltage between an output and input in this case is called the dropout voltage.
LDOs have a disadvantage, that they can be inefficient. Therefore input voltage for them should be set just above the bias point to ensure most efficient power supply. And that is the reason, why so many of them are employed. Every active element has its own LDO to decreases thermal noise of the particular regulator. They are in advantage of not having a switching element in them. Therefore, they are most suited for particular application. LDOs are also more effective than the other linear DC/DC regulator architectures. [23]

3.3 Reference oscillator

Reference oscillator is very important in frequency conversion chains. Its frequency is being up or downconverted, just as VCOs can be also. The same holds true for its noise.
Reference oscillator being used is TCXO from Raltron TX6100A-D3-5-100.000-5. Average spectrum analyzer being used as PN measuring

kit, shows its own noise floor (Figure 5), when it measures very good TCXO.
The shape of the output signal is also important. This proved an experiment with square and sinus 100 MHz reference oscillators. Only the sinus shaped one showed, that it was capable of stabilizing a VCO for -110 dBc @ 100 kHz offset from 9.2 GHz carrier. When square one was used, it managed only -106 dBc @ 100 kHz offset from the same carrier. Everything else was the same and the reference PNs were low enough. Measurements were all obtained with Agilent E4440 spectrum analyzer on 9200 MHz carrier. Simple explanation would be, that multiple harmonics were the cause. This investigation exceeds the scope of this work, but I think it is at least worth mentioning it in this case.

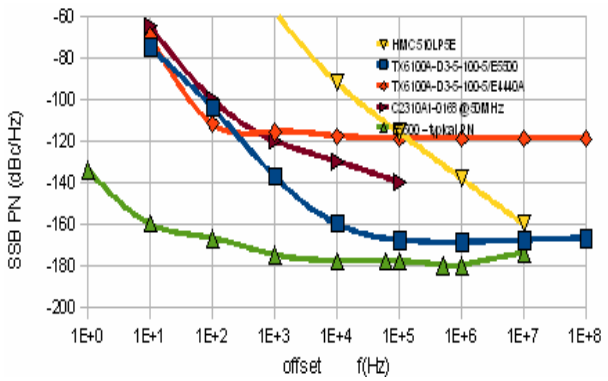

Figure 5. SSB PN measurement data of a 100 MHz TCXO TX6100A-D3-5-100.000-5 obtained with Agilent E5500 spectrum analyzer (Raltron).

Then there is an issue regarding oscillator drift. Frequency drift should be assessed beforehand, to set correct start frequency for an RMS PN measurement. Otherwise too high PN could result. If 100 MHz reference drifts at +/- 1 Hz/s, the 18 GHz oscillators output frequency would drift at +/- 180 Hz/s. And this drift could be caused by measurement setup as well. A compromise must be set, because measurement setup must follow this drift. Too fast drift can cause false readings.
One way to avoid this is to set a starting frequency of the E4440A span to 100 Hz and not at 10 Hz.
We can look at the PN influence from reference oscillator to the output signal as a transformation of frequency rise. That way it becomes clear, that output noise can get degraded by reference oscillator also. Therefore PN of a reference oscillator is also defined by the PN of the output signal from frequency conversion chain.

3.4 Local oscillators

The most important element in local oscillators are VCOs. They should be able to provide composite phase noise of about -110 dBc @ 100 kHz at the Tx output or IF Rx output. The shape of the PN function is important too, and it should be the one simillar to quiet oscillator (Figure 2). Of course input signal must be provided with a PN << -110 dBc @ 100 kHz, otherwise the test is invalid. The goal data for the PN test of the chain, follow from equation (6) and Figure 6. It is the data, that it should be tested against:

IF_Tx = 1390 MHz
PN << -110 dBc @ 100 kHz
Integrated PN ≤ -46 dBc

Actual frequency rise from reference oscillator was from 100 MHz. For receiving band (Rx) it was from 140 MHz to 18190 MHz. It was composed of bigger integer and smaller, but finer fractional frequency rises. At that, I am assuming a lower possible PN of integer PLL and a higher PN for fractional PLL. Integer PLL is being used as input/first oscillator in microwave part of the chain. Fractional on the other hand is being used in RF part for the frequency conversion below 1 GHz. Input IF of 1390 MHz is also being added to the output signal from microwave part of the chain. PN as uncertainty in a signal is being downconverted thruout the chain.

A goal of the research was to establish a connection between a VCOs PN and a PN from a frequency conversion chain. Figure 4 shows a part of the system recreated for that purpose.
RMS PN angle is usually measured in degrees and radians. Therefore it can be compared to values from Figure 3. It is also measured sometimes as jitter in (femto) seconds. On the other hand, EVM (Error Vector Magnitude) and CINR are a quick assessments of quality of radio link. Therefore they can be compared

to integrated PN value from Figure 6. They are composite parameters, therefore they show many characteristics rolled into one. They are measured in decibels and also do not only depend on PN.

We need something, that would describe receiver from its input onwards. Eb/N0 is defined to the input and not any further. At that, everything behind an input in a receiving chain is not taken into a consideration. But this chain behind input is critical for later digital processing. It decreases demodulator losses, if done properly. It also enables performances close to -1.6 dB to the Shannon limit (power efficiency). With that in mind, QPSK characteristic is within reasonable BER of 10^{-6} still > 12 dB distanced from Shannon limit for power efficiency of -1.6 dB. So treshold is the parameter to describe power efficiency. Its maximum values are also standardised for different digital modulations. For our case of 16 QAM, it would be as follows:

NF = 4.5 dB (noise figure),
R = 40 Mbps (transmission speed),
BW = 14 MHz (radio bandwidth)
and therefore:
Eb/No = 7.5 dB
Noise Floor = kT + BW + NF =
= kT + 71,5 dB + 4,5 dB = -98 dBm
C/I = X(BER=10^{-6}) - Noise Floor =
=-86 - (-98) = 12 dB (≈ Eb/No)

X is the receiving power for a 16QAM, 7 to 10 MHz BW input signal needed for bit error rate of 10^{-3} on 7 to 8 GHz radio. [30]

So, engineer developing an SDR system must have a way to assess a quality of finished radio link hardware in advance, l.s. as soon as in the laboratory alredy.

The ultimate test is a measurement of a signature, but it requires complete hardware and software solution in a laboratory. Therefore it is not a practical solution, when someone develops frequency conversion chains universally. [20]

It may seem the problem is in units, which are in dB or % for EVM (error vector magnitude) and CINR (Carrier to Interference Noise Ratio). So to establish a PN error contribution in EVM, its part has to be established.

Than it can be compared to actual EVM or CINR of the received signal in laboratory conditions. Formula for CINR (carrier to interference noise ratio) in an SDR system exists an is often used on the finished product. But it also does not give dependancy on PN only, therefore it is irrelevant here.

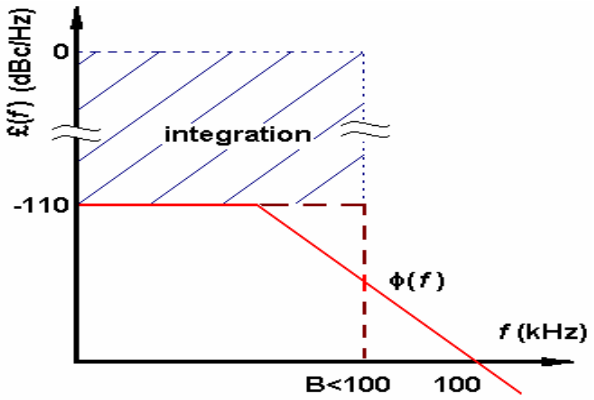

Figure 6. Defining equivalent effective bandwith for EVM calculation of (two stage) frequency conversion chain from £(*f*), which is expected SSB phase noise amplitude.

So to establish that connection one must rely on old and tried trial and error method, which is by far the most proven, but which defaults sometimes also.

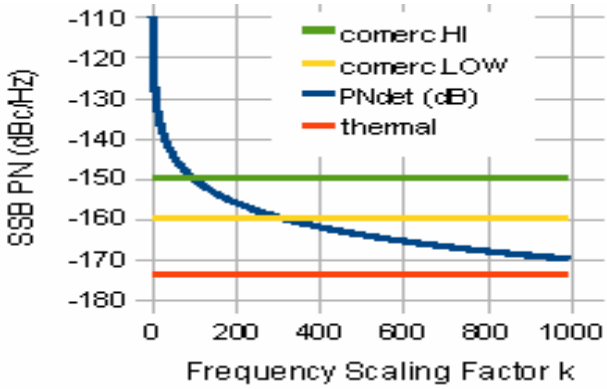

Figure 7. Back calculated theoretical deterioration PNdet(k) for 100 MHz reference oscillator. It is defined for -110 dBc @ 100 kHz at the output of 18 GHz frequency conversion chain. It is given against various natural and man made limitations. Theoretical rule can demand more performance, than nature or man can provide.

It must be said, that a form of a little bit of backward engineering is going on in this case. But it is almost all in the realm of the known data of PN spectrum. This form of noise prediction engineering can be done, when almost exact form of noise spectrum at the oscillators output is required for reliable operation. And it is also data based on previous experiences. Equation 6 gives integral value for SSB and DSB PN in dB,

which can be compared to CINR or EVM values. With calculated values a substantial security in the design could be obtained, as could be seen from later measurements. Equation (6) gives integrated value for SSB and DSB PN in dB, which can be compared to CINR or EVM values from measurement equipment. It can be seen, that reserve obtained can be substantial.
EVM reserve of some dB can come in handy later in the design stage, even due to very carefull planning of other quasi linear stages. These could produce some degradation in usefull signal along the chain, that would use up this reserve. It is very important, as available P_{1dB} is only that big at a certain device price and other constraints, as power supply,...etc.

$$\int_0^\infty \phi^2(f)df = \phi_0(f)B\frac{\pi}{2} =$$
$$= -100 + 50 + 2 = \quad (6)$$
$$= -48dB \quad (SSB)$$
$$= -42dB \quad (DSB)$$

$\phi(f)$ is a simplified PN function of the desired output noise and B is an equivalent bandwidth of this function in kHz. All local oscillators are controlled via SPI bus and µPc unit, which is located outside of oscillator unit. This SPI bus is silent, while frequency is not being changed. This is very important, as its 7 lines go right thru to the HMC700LP4E synthesizer chip.

Fref (MHz)	ref. PN (dBc@100 kHz) (required)
10	< -173.75
50	< -159.77
100	< -153.75
200	< -147.72
400	< -141.70

Table 1. Minimum back-calculated PN from equation (9) is rising for rising frequencies of the reference oscillator. It is needed for reference oscillator to achieve -110 dBc @ 100 kHz at the output of a frequency conversion chain.

Utmost care was also taken at designing the oscillator PCBs with the SPI bus. This is potentially the most powerfull single noise source in the VCO compartment of the oscillator housing.
Testing of the reference oscillator can be done in at least 2 ways. Both require spectrum analyzers. First is the direct method of measurement. This requires specialised extremelly low phase noise oscillators in spectrum analyzer, e.g. like Agilent E5052A Signal Source Analyzer. The second method does not require any such expensive specialised instrumentation. Just any standard spectrum analyzer, e.g. like Agilent E4440A, would do. With these staple measurement tools it can be done in indirect way. The reference oscillator frequency is upconverted in some way and then phase noise can be back calculated. This holds true for one point in the characteristics - usually at 100 kHz point. And this is the way we did it in this work.
Upper table gives examples of demanded PNs for different frequency reference oscillators. It is evident, that higher frequency reference oscillator needs not be so low noise as lower frequency counterpart. This is albeit that lower frequency TCXO can be made more easily and achieves lower PN in the process than higher frequency counterpart. The following familliar equations are giving some math behind the frequency conversion in balanced mixer. F_{OUT} is input frequency of the receiver (rx) but could be output frequency of transmitter also, interfrequency is output frequency of the receiver, but could also be input frequency of the transmitter (tx) chain and $f_{\mu W}$ is frequency of the microwave oscillator $F_{LO\#1}$. It is marked as first, because input signal is mixed with its frequency first.

$$F_{OUT} = 2f_{LO\#1} + F_{FLO\#2} - f_{IN} \quad (7)$$

Factor two is due to the fact, that a mixer with the doubler was used (Figure 14). Relevant connection to the reference oscillator gives the following equation for complete frequency conversion factor *k*. It is needed for theoretical factor calculation in Figure 7.

$$k = \frac{F_{OUT}}{F_{REF}} \quad (8)$$

Figure 7 gives $PN_{REF}(f_0)$, which is required PN for reference oscillator in one point according to desired F_{OUT} and its £(f) function (Figure 6).

$$PN_{REF}(f_0) = PN_{OUT}(f_0) - 20\log\left(\frac{F_{OUT}}{F_{REF}}\right) \quad (9)$$

where: $f_0 = 100kHz$ (offset)

Theoretical factor of deterioration or improvement on PN is given as (10):

$$\mathrm{PN}_{\mathrm{deter./improv.}}(f_0) = \pm 20\log(k) \quad (10)$$

Output $PNout(f)$ is closely following the noisiest VCO in a chain. In multi VCO chains, the noises are being added. In any case the equivalent $VCO_{PN}(f)$ must follow the £(f) function (Figure 6).

$$PN_{OUT}(f) = £(f) \quad (11)$$

X gives division factor for the VCO prescalers in PLL synthesizer. N and R are frequency ratios for adequate oscillator.

$$X = \begin{cases} \mathrm{N};\ \text{integer PLL}, \\ \mathrm{R};\ \text{fractional PLL} \end{cases} \quad (12)$$

Forseen value of -110 dBc/Hz is noise power spectrum density for equivalent oscillator. It is the same value as noise power spectrum density in a point at the offset 100 kHz from the carrier, so further calculations can be easily made. Another thing that must be forseen, is the shape of the equivalent oscillator output noise spectrum. Simplified shape of the "healthy" oscillator is forseen, as it should be the case in a real circumstances. This "healthy" status is determined by the phase noise of another "healthy" low noise oscillator, not neccessary another chain. Figure 6 gives such a power spectrum based on the real systems.

Noise power spectrum density can be recursively calculated for the wanted final EVM (Error Vector Magnitude) value from many iterations. Some reserve should be taken into account for nonideal nonlinear elements in the chains. These are primarily high frequency transistors, mixers and amplifiers. Equation (9) gives only the last calculation for our system. From it, it can be seen, that just by choosing the ultra low noise VCOs, a 10 dB reserve for EVM (error vector magnitude) can be achieved in the frequency conversion chain.

Calculation can be done in this way because we assume all PNs from all oscillators come together in one single output PN function £(f). And with that fact true, an integration calculation can be done on the simplified shape $\Phi(f)$ of a spectrum £(f). Figure 6 gives simplified noise spectrum equivalent bandwidth. It is less than required in real circumstances. It can be done because:

- we only look at the absolute sum of the phase noise. It is also the case in EVM (error vector magnitude) and CINR (carrier to interference noise ratio), so we can compare it,
- the scale is logarithmic, so the characteristic is not linear as assumed in the graf.

3.5 Synthesizer

The HMC700LP4E is a SiGe BiCMOS fractional frequency synthesizer. PLL synthesizer chip HMC700LP4E is intended for integer as well as for fractional PLL operation. The synthesizer includes a very low noise digital phase frequency detector (PFD), and a precision controlled charge pump (Figure 8).

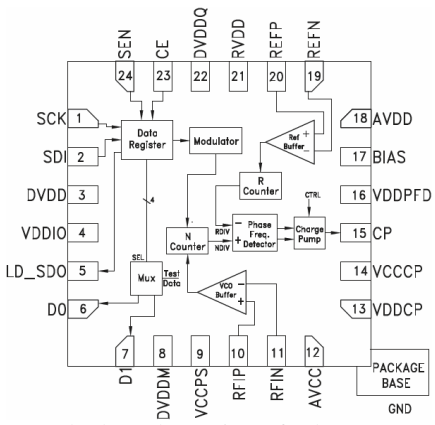

Figure 8. Block schematic of the HMC700LP4E synthesizer chip [9]

The fractional synthesizer features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and very low spurious products. This feature is something I tried to take an advantage of, to acheive low phase noise (PN) in fractional application. [9]

The HMC700LP4E phase-frequency detector (PFD) features cycle slip prevention (CSP)

technology. It also allows ultra fast frequency hopping times. CSP feature would also (hopefully) help decrease a number of phase pops and slips in the temperature chamber, but it was not tested in this case. [9].
PLL loop is based on the HMC700LP4E phase detector with no external prescaler at the input, as the Hittites VCO HMC510LP5E alredy contains divide-by-2 and divide-by-4 outputs.
Charge pump output of the HMC700LP4E chip loops PLL loop together with filter (4th order). Filter must provide phase noise < -110 dBc @100 kHz for the single oscillator and < -115 dBc @ 100 kHz at divided output RF/2. PN at the output of the complete Rx chain should also be -110 dBc @ 100 kHz offset.
Matched filter at the output of a local oscillator is not neccessary. Unwanted harmonics of 3f, 3f/2,... etc [7, 8] must be suppressed enough so that they do not interfere harmfully in the mixers or even in the oscillators themselves, so that stability of the oscillators can deteriorate. Order of this filter should be dependant mostly on number and amplitude of unwanted harmonics. The LP (low pass) filter in oscillator built around V585ME58-LF hybrid was based on 5th order stepped line design.

3.6 Active filter for PLL loop

A choice of active PLL filters operational amplifier was also considered in detail. It is unavoidable for VCO tune control. Possibility of power supply voltage > 20 V must be kept open, when choosing one. It should also have good power supply noise rejection for this application.
VCOs used in this application utilize higher than 5 V tuning voltage range - in fact, it is up to 10 V. This is good, because inbuilt varicaps tend to generate less noise at higher voltages. This is so despite danger of avalanche noise at too high a tuning voltage. But it also worsens a noise conditions at overshooting the designated absolute maximum V_{tune} for the VCO. This kind of active filters would then be generating more noise indirectly due to operational amplifier output noise source.
Several operational amplifiers were considered for the application. An AD797ARZ was chosen for an AMP in the LPF aplication as it was found to be most compatible with a low PN goal. This operational amplifier is designed specifically with PLL LOOP amplifier in mind. It has so little restrictions regarding operation, that it is entirely up to the designer, how far one dares to go with the PLL design. This IC is designed for extremely low noise operation and not much else seemed to matter at the conception of it. This is the concept I deem correct for this application.

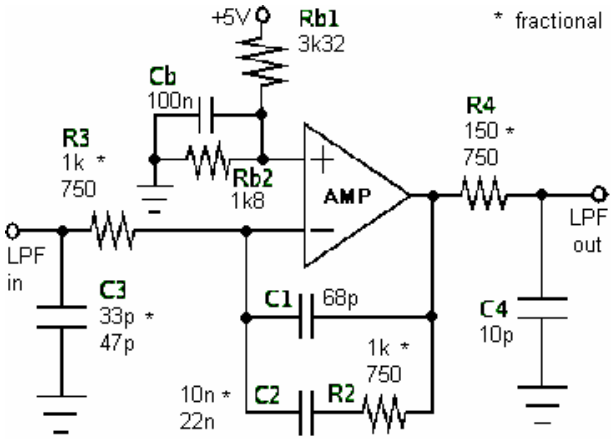

Figure 9. Topology of the 4th order active low pass filter (LPF) used in integer and fractional PLL loop. Phase margins were 65° and 55° for integer and fractional PLLs

Of course much depends on the chip manufacturer daring to announce the lowest power consuption, noise, highest output power available,... etc. All these parameters were deciding factors for choosing between all the candidate synthesizer chips from rival chip manufacturers.
Final deciding parameter was a possibility of the very high phase detector frequency.
This is so, because then a higher reference frequency could be used. Higher reference frequency ensures lower overall output phase noise due to multiplication issue. Higher phase detector frequency also enables wider loop bandwidth, which ensures quicker lock times in case of phase clicks and pops [19]. The latter are especially an issue, when we expose a system to relatively quick temperature changes, e.g. in temperature chamber or deployed on the field.
Filter for N-PLL might even work for fractional PLL. Actually it can be achieved better level of performance in N-PLL with low pass LOOP filter designed for fractional PLL, but it would then be restricted to only certain frequencies. That is why this concept of

designing was abandoned. This information is important as most new chips are designed for dual operation. Integer PLL operation is prefered before fractional, as lower PN can be achieved. There are also other benefits, that consider higher speeds of operation with integer PLL. Either of the modes can be set at any time of synthesizer operation.

3.6.1 Integer PLL oscillator

This oscillator is previously mentioned microwave (μW) oscillator. VCO for integer PLL oscillator operation is HMC510LP5E, which is onchip voltage controlled oscillator for better PN performance. It also has divide-by-2 and divide-by-4 outputs for direct interfacing into synthesizer chip.

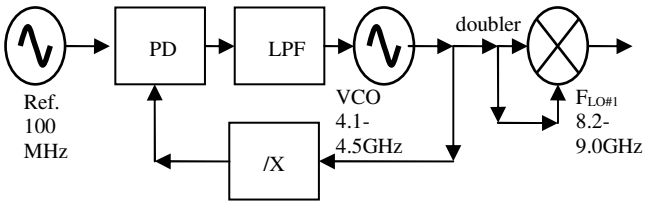

Figure 10. Block schematic of the LO#1. It is made of an integer PLL stabilized VCO. HMC700LP4E synthesizer is shown simplified with PD and multiplier (/X) blocks. Another doubler at the end of this chain is a part of the mixer chip in a mix#1 block [10].

MMIC VCO in a leadless housing is built in a GaAs InGaP Heterojunction Bipolar Transistor (HBT) technology. It was chosen due to working environment in which it was supposed to work and integrates resonators, negative resistance devices, varactor diodes and features divide-by-2 frequency and divide-by-4 frequency outputs. The VCOs phase noise performance is excellent over temperature, shock, and process due to the oscillators monolithic structure. Power output is typically +13 dBm from a +5 V supply voltage. The prescaler and divide-by-4 functions can be disabled to conserve power, if not required. The voltage controlled oscillator is packaged in a leadless QFN 5x5 mm surface mount package, and requires no external matching components. [7]

A frequency step for this oscillator is 200 MHz. Integer operation of the HMC700LP4E synthesizer chip for PLL oscillator is chosen for its better PN performance. PLL bandwidth is maximized due to expected much better response to microphony. 150 kHz of bandwidth is allowed with 100 MHz PFD frequency. This is where this outstanding characteristic comes onto its own.

Figure 11 shows simulated results for HMC510LP5E VCO stabilized with integer PLL and realised with the HMC700LP4E synthesizer chip.

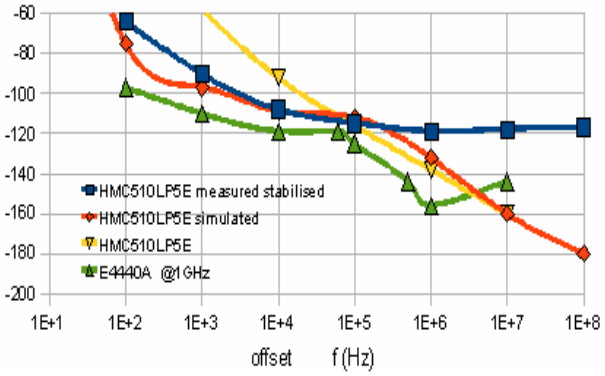

Figure 11. SSB phase noise for HMC510LP5E at various stages of design and against measurement instruments SSB phase noise

Measurement results show (Figure 11) improvement of actual VCO phase noise due to the integer PLL stabilization. They agree with the simulation results from Hittite simulator. According to PN measurement output PN of less than -110 dBc/Hz @ 100kHz can be expected. This is so because this oscillator produces half of the frequency for the mixer. When it is raised by two in the mixer again, a PN would be increased by 6 dB acccording to theoretical rule. Therefore composite noise would be arround -104 dBc/Hz @ 100 kHz offset.

3.6.2 Fractional PLL oscillator

Fractional PLL mode of operation was chosen for the RF oscillator. Its output frequency $F_{LO\#2}$ covers 1,43 to 1,83 GHz band for IF#1 downconversion from 1.39 GHz ±100 MHz to IF#2 at 140 MHz. Its very low PN of -123 dBc/Hz @ 100 kHz makes it ideal for the purpose, which makes PN of the whole downconversion system dependant only on the PN of the first LO#1. VCO chosen for this oscillator is a VM585ME58-LF from Z-comm. It is a hybrid VCO in a leadless QFN 15x15 mm surface mount package, and requires no external matching components. [8] It

integrates resonators, negative resistance devices, varactor diodes and features a single output. The VCOs phase noise performance is excellent over temperature and shock. Power output is + 6 dBm typical from a +10 V supply voltage.
This very low noise also provides some backup reserve for the notoriously higher levels of noise from fractional PLLs. Figure 10 shows the oscillator block chain used to stabilize this VCO.

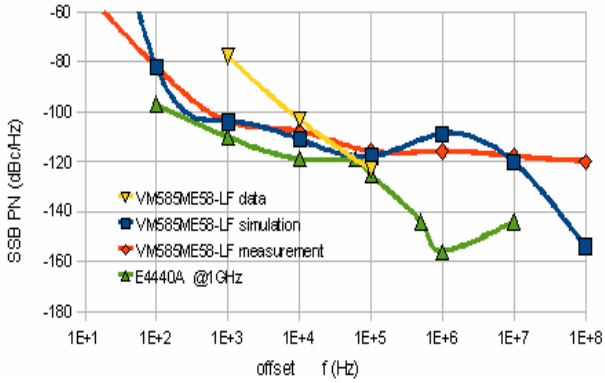

Figure 12. SSB phase noise for V585ME58-LF at various stages of design and against measurement instruments SSB phase noise

According to manufacturers data, a PN of less than -123 dBc/Hz @ 100 kHz could be achieved. This means, that when this noise would be summed with the noise from the microwave oscillator, it would not contribute at significant level. Due to a higher phase margin, a PN of the stabilised fractional oscillator is expected to be a little bit higher than manufacturers data. Therefore a microwave oscillator would stay the main contributor to the composite PN of the chain.

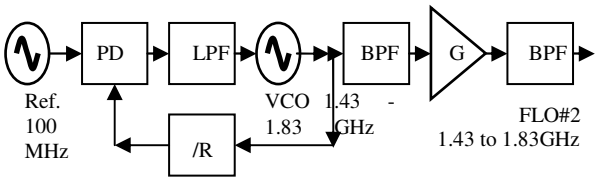

Figure 13. Block schematic of LO#2 made of VCO stabilized with fractional PLL. HMC700LP4E synthesizer is shown simplified with PD and divider (/X) blocks [9]

A frequency step for this oscillator is 125 kHz. But it can actually be set at a much higher resolution of 5 Hz, which was not the goal. Fractional operation of this PLL oscillator is chosen for its better PN performance due to much higher PD frequency that this mode of operation can provide according to very small frequency step, that is required at the output.
Even this high resolution does not deteriorate low PN operation of the fractional PLL. It has inbuilt 3rd order Δ-Σ modulator. This state of the art device does not add much PN as other fractional synthesizer chips from other manufacturers do. Measurement results show (Figure 12) deterioration of actual VCO phase noise due to fractional PLL stabilization. They agree with the simulation results from Hittite simulator.

4 PN of a microwave chain

From the measured oscillator PNs can be calculated, that PNs @ 100 kHz offset of the output signal can be around -110 dBc. Figure 17 shows a measurement of the output PN, that confirms the assumption. This figure also confirms RMS degree measurement, which is integrated PN, to be less than demanded maximum angular error for 256QAM in Figure 3. Figure 19 shows the CINR measurement of -36 dB in the system under lab conditions. This should be good enough for reliable operation, which is given in Error Free Seconds (EFS).

4.1 Input signal characteristics.

Figure 16 shows a PN of an input signal. It was obtained from Agilent sinus source E8257D. Measurement was done with E4440E spectrum analyzer and compared with original manufacturers data obtained from instrument manufacturer. As we can see, sinus source is almost as good (or even better) as a measurement instrument, so its PN closely follows its noise floor. [13]

4.2 PN design concept for a chain

Phase noise is always 3 dB higher in cascaded frequency conversion chains, where equal PNs are being summed. The reason is that white noise signals are not correlated, in fact their autocorelation functions are 0. Otherwise PN of the noisier VCO prevails. This is regardless of whether chain is up or downconverting.

4.2.1 First downconverter

First downconverter is composed of first mixer and the integer oscillator for better PN performance. It is realized with the HMC570LC5 chip (Figure 14), which is a compact GaAs MMIC I/Q downconverter in a leadless RoHS compliant SMT package. This device provides a small signal conversion gain of +10 dB, a noise figure of 3 dB and 18 dB of image rejection across the frequency band. The image reject mixer decreases the need for a filter after the LNA, and removes some of the unwanted thermal noise at the image frequency.

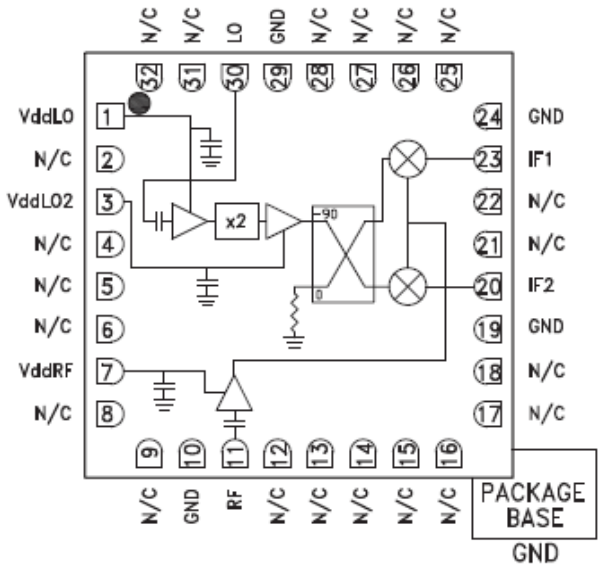

Figure 14. The HMC570LC5 is a compact GaAs MMIC I/Q downconverter in a leadless RoHS compliant SMT package. [11]

I and Q mixer outputs are provided. An external 90° hybrid is needed to select the required sideband. The HMC570LC5 is a much smaller alternative to hybrid image reject mixer downconverter assemblies. [11]

4.2.2 Second downconverter

First downconverter is composed of first mixer and a fractional oscillator for better PN performance. The mixer is an HMC316MS8E chip. It is a passive GaAs schottky diode mixer, which makes planar on chip balun transformers. It requires no external components (Figure 15)

A mixer from this application is used as a frequency downconverter. HMC316MS8E is used as an RFIC downconverter from 1.39 GHz to 140 MHz. At mid-band, a mixer provides 7.5 dB conversion loss and a +25 dBm IIP3 with LO drive levels of +19 dBm. The mixer design was optimized for low cost high volume applications where high linearity of frequency converter is required. [12]

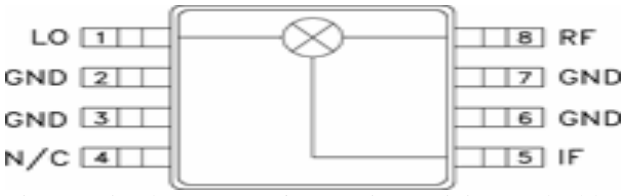

Figure 15. The HMC316MS8E is a miniature double balanced mixer in an 8 lead plastic surface mount package [12]

4.3 PN measurement results for frequency conversion chain

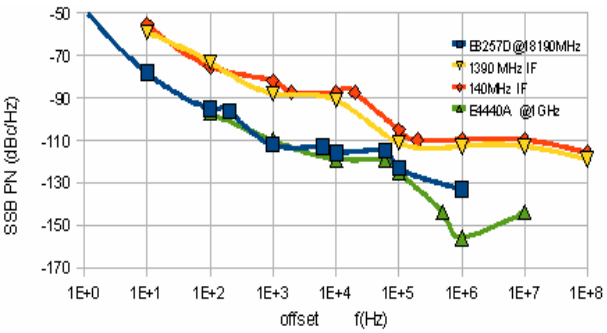

Figure 16. SSB PN measurement of the IF from the first downconverter to the last, obtained with E4440A spectrum analyzer.

Figure 16 shows measurement result for output SSB phase noise of 140 MHz carrier. The result agrees with the prediction result at 100 kHz offset and general shape of the PN function. PN is not -110dBc/Hz @ 100 kHz, but rather -105 dBc/Hz @ 100 kHz due to frequency doubling in HMC579LC5 downconverter. Phase noise is well within the limits for 256 QAM modulation (Figure 3).
Figure 18 shows chain during measurement phase. Numbers 1 and 2 are first and second downconverter blocks, 3 is N-plexer circuit, which is entirely passive. It consists of various filters for rx/tx interfrequency separation, which do not contribute to output PN of 140 MHz carrier. Figure 19 shows constallation diagram test for 256 QAM signal. Input level was -40 dBm, which is nominal value for assuring of a good BER deployed microwave radio operating conditions.

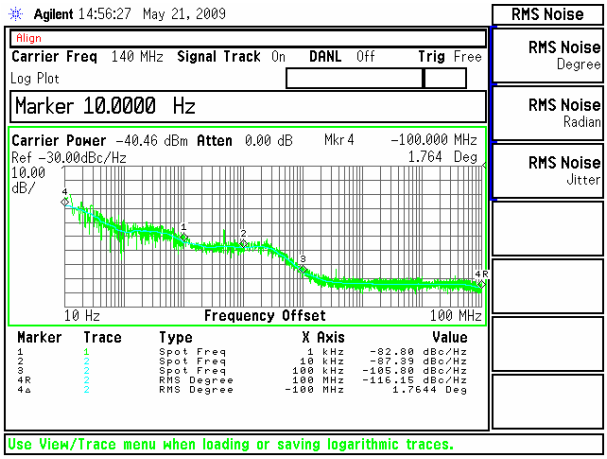

Figure 17. SSB PN measurement of the 140 MHz IF from the second downconverter obtained with E4440A spectrum analyzer. It shows integrated PN well within the limits for 256 QAM modulation (Figure 3).

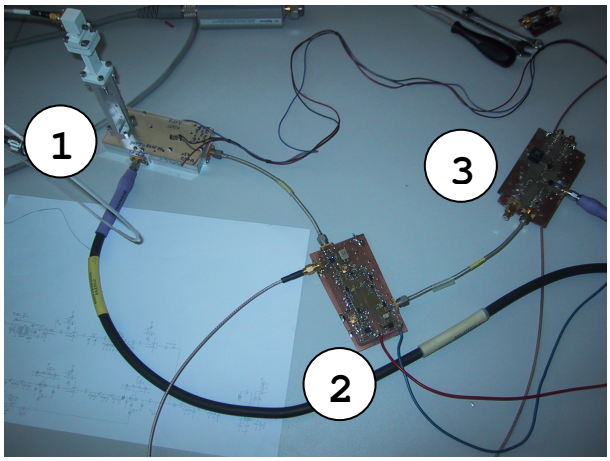

Figure 18. System during measurement for constellation diagram and PN. 1 and 2 are first and 2nd downconverter. 3 is N-plexer, which is passive circuit.

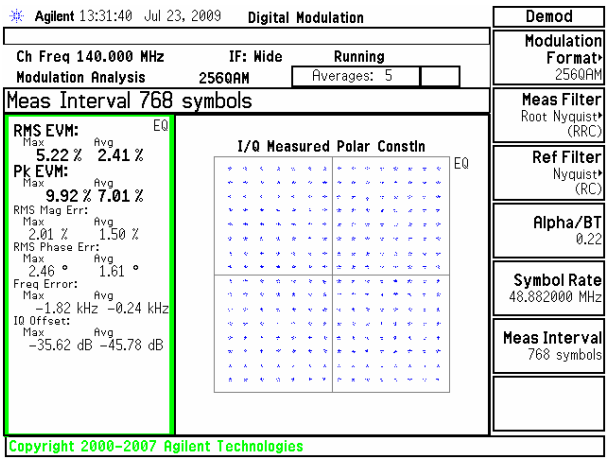

Figure 19. shows measurement result for constellation diagram at 256QAM and 56 MHz bandwidth (365 Mbps), obtained with E4440A spectrum analyzer. Maximum EVM is around = -36 dB, shown by the SDR equipment itself.

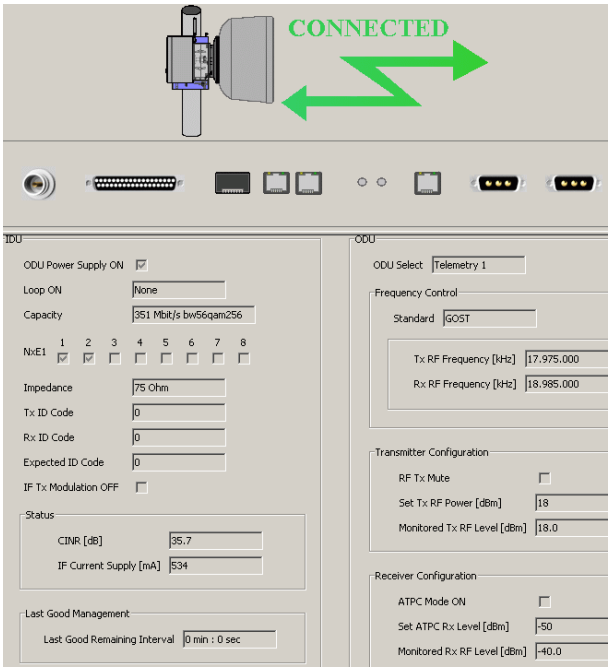

Figure 20. Telemetry data from one radiolink system in full configuration during practical PN bench test of the frequency conversion chain.

5 Conclusion

In order to change a frequency of the input carrier we always gain more of the phase noise. Heterodyning chains are showing a conversion factor for deterioration of PN, when upconverting or downconverting a reference or VCO frequency. Three dB are gained on PNin a chain, when 2 of the same strength signals are summed. So the best approach to building these chains is to select the best oscillators, providing that high enough dynamic range of the amplitude is provided. In the subsequent stages, designer must be very carefull not to loose any of the very good PN from the reference oscillator and VCOs, thru the amplitude conditioning of the various quasilinear components. Achieved -105 dBc/Hz @ 100 kHz offset deviates from targeted -110dBc/Hz @ 100 kHz. But it also shows, that at least reference TCXO may not need to be -153 dBc/Hz @ 100 kHz offset, and could be more noisy for the same effect.

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