Agilent EEsof EDA GoldenGate

The Solution You Asked For

The proliferation of wireless communications drives the need to design complex RF integrated circuits. The RF circuit designer is faced with the challenge of meeting rigorous specifications and completing designs within a narrow development window. To address these demands, RFIC companies must adopt a Best Practices RFIC design methodology that addresses full characterization of the radio before tape out and optimization of the radio for high yield production.

Agilent's GoldenGate Simulator provides unique frequency domain analysis facilitating this Best Practices methodology. As such, GoldenGate users reduce costly design spins, increase manufacturability and reach their design goals while minimizing project risk.

Agilent Technologies

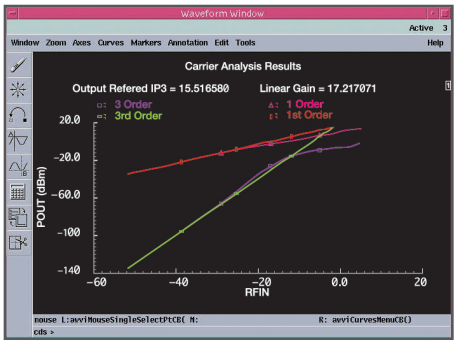
GOLDENGATE BENEFITS

- Full radio verification for entire RFIC with actual digitally-modulated signals.
- Advanced automated analysis such as EVM, ACPR, Gain Compression, IP3 and nonlinear noise.
- Comprehensive load-pull characterization.
- Quickly converge on high-Q and crystal oscillators.
- Efficient simulation of fully-extracted views.
- Complete Monte Carlo, corners and yield analysis for design centering.
- Seamless integration with Cadence® Analog Design Environment.
- Silicon-accurate simulation with industry-standard Spectre™ PDK.

UNIQUE RFIC VERIFICATION

GoldenGate's unique algorithms are optimized for the challenging demands of modern complex radio design. These demands require a simulator with capabilities not previously available. GoldenGate addresses these demands with the ability to converge on complete transceivers with the speed to enable full characterization prior to tape out.

MIXER ANALYSIS

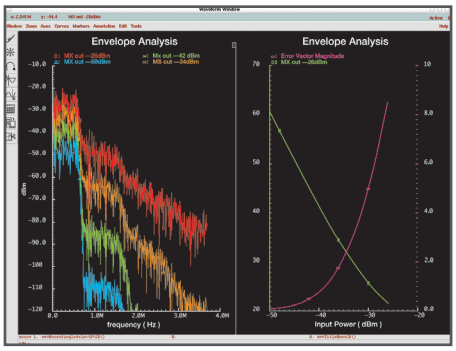


IP3 for low-IF mixer

Mixers are the fundamental block for upconversion or downconversion of signals in a transceiver. GoldenGate efficiently analyzes the effects of this frequency translation by accurately measuring the conversion gain, noise figure (with and without blocking signals), small signal noise, linearity (IP2/IP3) and spurious responses. Furthermore, modern low-IF architectures require the LO and carrier frequencies to be very close together. GoldenGate's harmonic-balance capabilities allow the designer to automatically calculate these metrics far more efficiently than with traditional transient techniques.

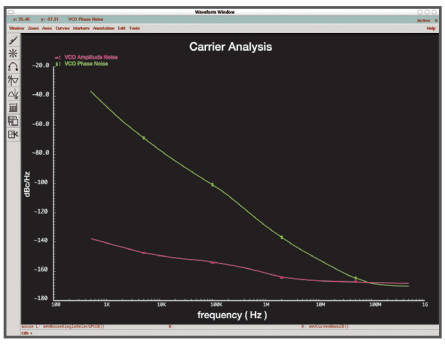
AMPLIFIER ANALYSIS

Amplifiers have a wide range of applications, each requiring specific design tradeoffs. GoldenGate provides the ability to properly analyze linearity, gain and efficiency through automated analyses such as IP3/IM, large signal S-Parameters, Pin-Pout, Gain Compression, PAE, ACPR, and EVM. Traditional two tone analysis is, at best, an approximation to reality and does not offer the designer complete characterization of the amplifier. GoldenGate's Envelope Transient technique provides the necessary capability to simulate actual digitally-modulated signals, giving a real-world representation of the performance prior to tape-out.



Accurate ACPR and EVM of QPSK modulated signal for CDMA receiver

OSCILLATOR ANALYSIS

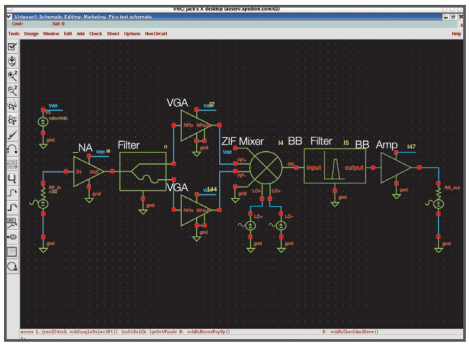


VCO phase noise and amplitude noise sweep

Oscillators are used extensively in both receive and transmit paths. Oscillators are particularly susceptible to noise, specifically phase and amplitude noise. Nonlinearity and periodic variations in both the LO and signal path create difficulties for traditional time-domain simulators. GoldenGate's Envelope Transient and Harmonic Balance approaches enable a much faster and more accurate analysis of

startup conditions, oscillation frequency, total harmonic distortion and phase noise. Additionally, GoldenGate simulates oscillator and divider combinations and high-Q oscillators efficiently.

FULL TRANSCEIVER ANALYSIS



Direct-Conversion CDMA receiver

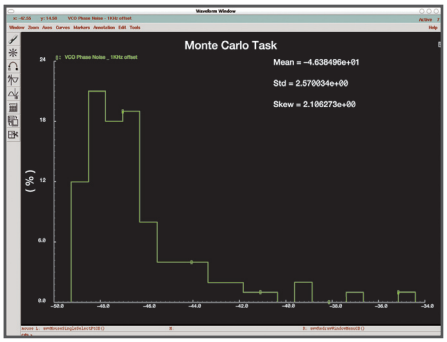
Separate analysis of the RF building blocks is necessary but not sufficient. A complete RF to baseband analysis of the entire chain is the only way to determine whether your radio will perform. GoldenGate's capacity and convergence give designers the ability to simulate the entire chain to fully characterize block interaction, noise propagation effects and specification conformance. The capability to do advanced parametric sweeping enable the designer to make intelligent design trade-offs earlier in the design cycle. GoldenGate's proven convergence has successfully simulated transceivers in excess of 10,000 active devices, enabling true full-radio characterization.

PARASITIC EFFECTS

Parasitic elements can degrade circuit and noise performance by over 5db. Though often overlooked, simulating with extracted views is a crucial step to ensure working silicon. GoldenGate's frequency-domain analysis enables hundreds of thousands of passive parasitic elements to be simulated, driving down design spins.

INCREASED MANUFACTURABILITY

Designers are often faced with the task of not only designing a working radio, but ensuring it is highly manufacturable in volume. GoldenGate enables the designer to run extensive Monte Carlo analyses, sweeps across process corners and yield analysis. GoldenGate also provides the capability to simulate many design trade-offs through advanced optimization. These simulations have traditionally been too time consuming to be useful given tight design schedules. GoldenGate enables these important analyses by providing simulation speedups orders of magnitude over traditional transient-based techniques.



Monte Carlo histogram for phase noise of VCO at 1Khz offset

REDUCED PROJECT RISK

GoldenGate is completely integrated into the Cadence Analog Design Environment, including setup, waveform viewing, back annotation, scripting and most test benches. GoldenGate also directly parses the Spectre™ Process Design Kit (PDK) from all leading foundries. GoldenGate's foundry-proven success combined with the capabilities not previously available to the designer guarantee lower risk in getting your RFIC to market quickly.

COMPLETE MODEL SUPPORT

- MOFSET models including: PSP, BSIM1, 2, 3 (3.2.1 – 3.2.4), 4, MOS902, 903, MM1100, 1101, EKV, HISIM
- Bipolar Junction Transistor (BJT) models including: VBIC, HICUM, MEXTRAM, HBT and Gummel-Poon
- GaAsFET models including: CURTICE, STATZ, TAJIMA, TOM1, 2, 3
- Both Schottky Barrier and junction diode models
- Extensive models for microstrip, stripline, coupled, coplanar, susupended and finline structures.
- Comprehensive built-in user-defined sources for QAM, QPSK, chirp, and noise.
- Verilog-A support & bsource

SUPPORTED PLATFORMS

- Linux
- Sun/Solaris
- HP-UX (GUI)

Contact your Agilent EEsof EDA field sales engineer for more information about EMDS or for a free evaluation.

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