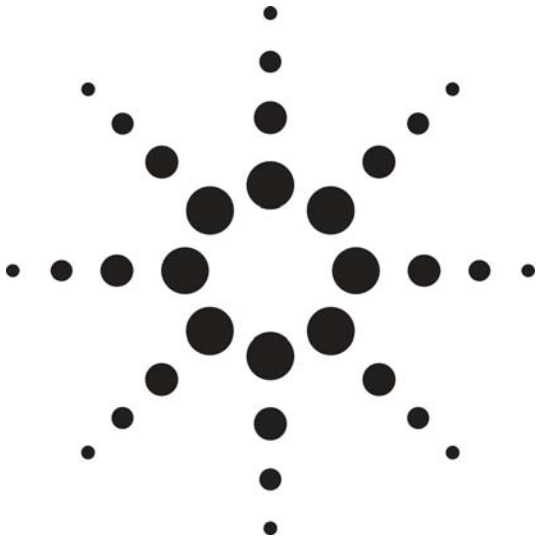


Signal Integrity Design Solutions in Advanced Design System

Technical Overview

Preliminary

Signal Integrity Designer bundles are Advanced Design System Signal Integrity design solutions that provide the most advanced simulation and verification technology available today for high-speed digital link designs. They provide designers:

- The ability to analyze complete digital links
- Jitter diagnosis, resulting in dramatically reduced product design cycles.
- Confidence that BER simulation results will match measured performance.
- The ability to allow calibrated modifications to high-speed data links to obtain the best possible performance.

Signal integrity is a major concern for engineers doing high-data-rate designs such as Infiniband, PCI Express, RapidIO, and 10 Gigabit Ethernet. Increasingly fast circuits with high clock speeds are in demand, and meeting this requirement is a constant challenge for every digital designer. High-frequency analog effects such as reflection, cross talk, ground bounce, and propagation delays through interconnects adversely affect signal quality and timing performance. Signal Integrity Designer Premier has the right simulation tools and libraries, including a multi-layer interconnect library that enables you to accurately model and analyze high-speed interconnect problems before fabrication, resulting in lower development costs and faster time to market.

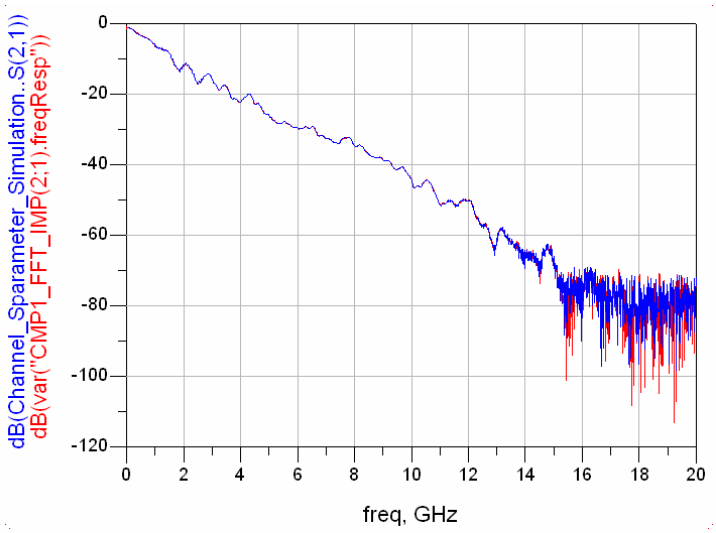
With an architectural shift from parallel link to serial link design, digital board designers are facing design challenges due to increased data rate and throughput requirements. Modeling a communication link requires integration of complex SERDES models to recover a digital signal at the receiver end. The performance of a high-speed serial link is evaluated chiefly in terms of its eye diagram performance and BER performance at the receive end. If the eye diagram response is not acceptable, signal processing techniques such as pre-emphasis and equalization are used at the transmit and receive ends to improve signal quality and timing performance.

Agilent Technologies

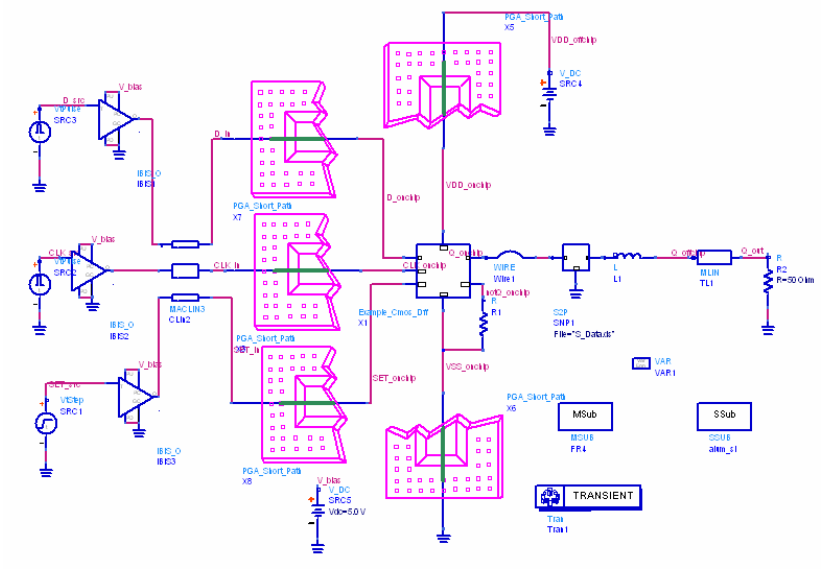
High Frequency SPICE with Convolution Simulator

At data rates exceeding 1GBps, the only way to characterize interconnect models are in terms of their S-parameter measurements. The measured data must be simulated with a time-domain simulator to provide eye diagram or BER channel performance. Designers can use the Broadband SPICE Model Generator to convert measured or modeled S-parameter models into lumped SPICE models or pole/zero models, but this method may have serious limitations for electrically long transmission lines, backplane, or noisy S-parameters. The convolution simulator is a preferred approach to analyze S-parameter models using time-domain simulation.

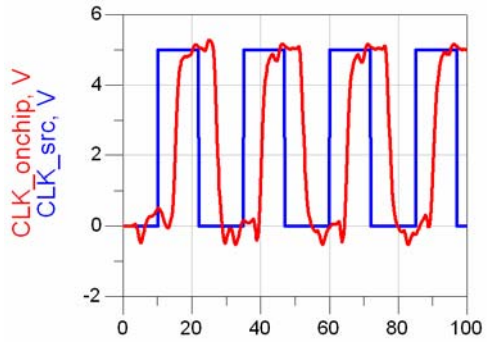
Convolution simulation operates by taking the impulse response of the frequency-domain interconnect models and convolving it with the input digital signal to accurately predict time-domain performance. It takes into account high frequency effects such as skin effects, high frequency dispersion, and dielectric losses that are associated with high frequency transmission lines. The advanced convolution technology in ADS (patent pending) provides several powerful techniques for causality correction, delay causality enforcement, passivity enforcement, and optimal techniques for frequency response preservation. The convolution simulator in ADS works transparently with High frequency SPICE and enables concurrent simulation of non-linear transistor level devices with S-parameter models.



Comparison of 10 Gb measured backplane S-parameters with S-parameters derived from the ADS convolution simulator.



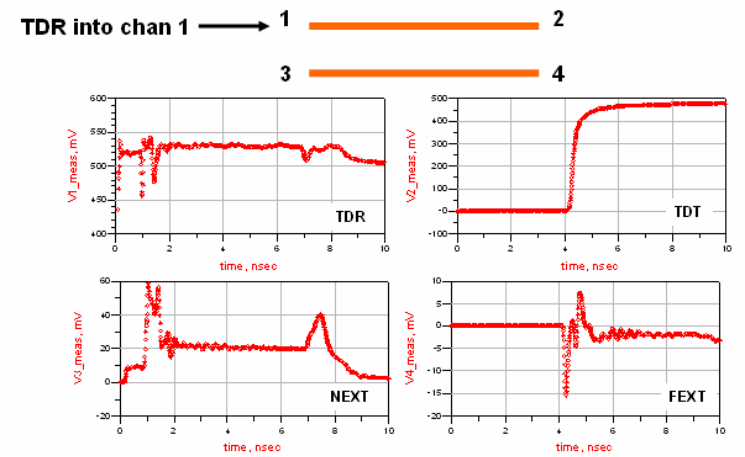
The schematic shows the time domain simulation of IBIS models, package, and nonlinear transistor devices based on ASIC and S-parameter models.



An on-chip time domain waveform.

Time Domain Reflectometry and Transmission (TDR/TDT)

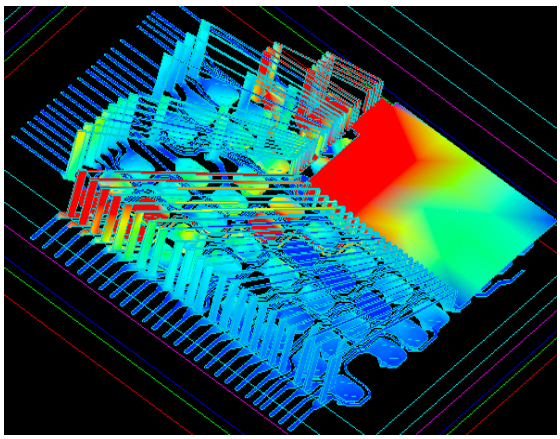
Time Domain Reflectometry consists of sending a voltage step down a line and comparing the incident and reflected voltage waves. The shape and polarity of the reflections tells the position and nature of each discontinuity. The ADS High Frequency SPICE simulator with convolution is highly accurate for simulating TDR/TDT response.



The TDR/TDT response a 2.5 Gbps differential channel.

Momentum is a 3-D planar electromagnetic (EM) simulator used for accurate interconnect analysis. It accepts arbitrary design geometries (including multi-layer structures) and accurately simulates complex EM effects including coupling and parasitics. Accurate EM simulation enables signal integrity designers to improve interconnect performance and increases confidence that the manufactured product will function as simulated.

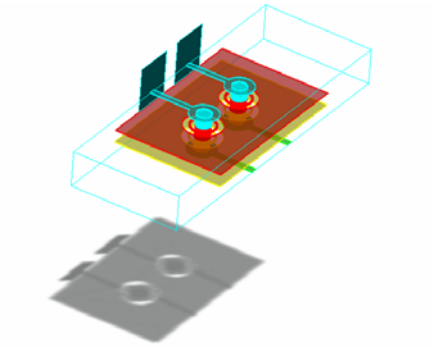
Momentum RF is a second solver technology within the Momentum EM engine that reduces simulation time without sacrificing accuracy on large and complex structures.



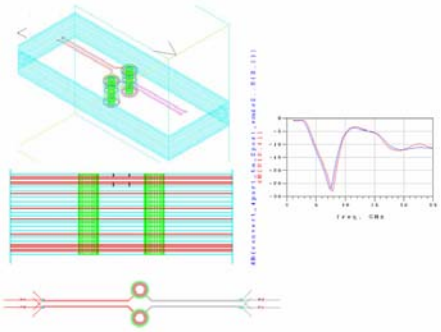
Accurate coupled via-hole simulation using Momentum.

Electromagnetic/circuit co-simulation with layout components breaks down the barriers between electrical and physical analysis domains. The layout component technology allows ADS users to create layout components that can be used in the schematic design environment. Once artwork and ports are defined, the user can generate a layout component with the click of a button. Because Momentum is integrated into the ADS design flow, simulation setup times are reduced, and design productivity is increased.

Electromagnetic Design System (EMDS). There are many types of physical layout components such as high speed connectors, bondwires, and dielectric bricks that require three-dimensional electromagnetic analysis for any arbitrary geometry. ADS provides an integrated finite element analysis tool called EMDS. Designers can import a layout from another layout tool and simulate it using either the 3D planar EM engine based on Method of Moments (Momentum) or EMDS, the 3D engine that is based on Finite Element Analysis.



3DsSimulation of a coupled via.

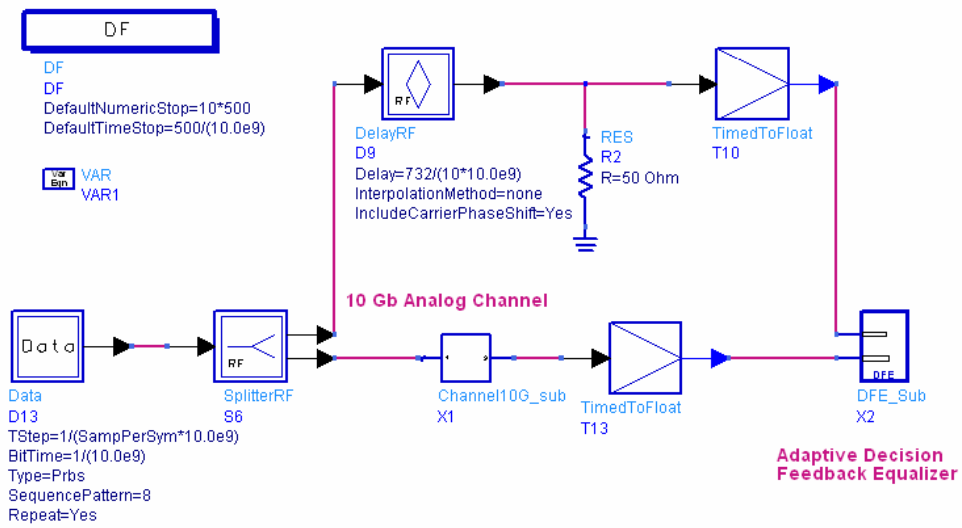


Comparing coupled via results-- Momentum and EMDS

Link Level Simulator in Signal Integrity Designer Premier

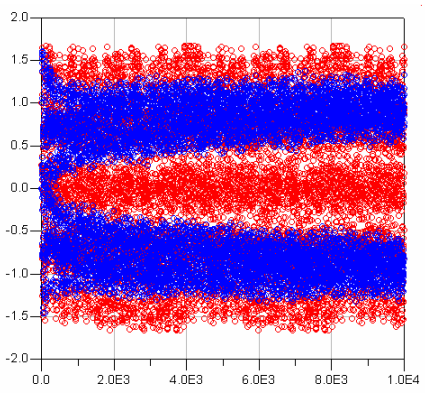
The link level simulator in ADS simulates digital signal processing components such as SERDES models consisting of FIR-filter-based pre-emphasis, non-adaptive and adaptive equalizers such as Feed Forward Equalizers and Decision Feedback Equalizers. The Agilent Ptolemy simulator is ideal for serial link simulation because it provides the ability to co-simulate DSP components in a link with analog and RF components and provides a true mixed-signal environment. The analog/RF components could be linear components such as S-parameters or nonlinear components such as transistors and IBIS models.

Agilent Ptolemy also allows designers to include the physical components imported from other back-end layout tools into the analog environment to perform link-level analysis. ADS provides powerful jitter analysis capabilities and provides excellent correlation between simulated and measured jitter components and BER measurements. ADS Ptolemy allows integration of MATLAB intellectual property (IP) into the channel path for co-simulation with Ptolemy, analog, and other EM based components. Designers also can represent part of the serial link as System-C, C++ , and Verilog-A-based behavioral models.

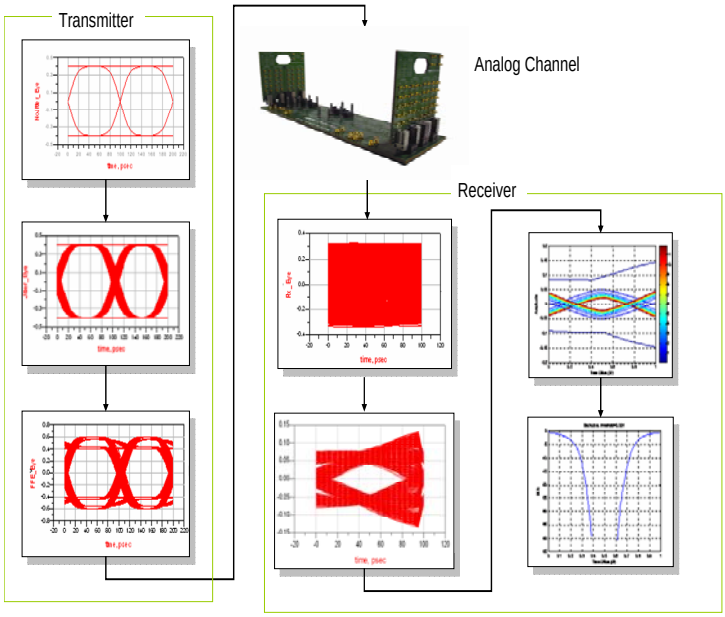


System level co-simulation combines the analog channel with adaptive equalizers.

ADS provides system components such as 8B10B coders/decoders, 64B66B coders/decoders, FIR filters, PRBS sources, FFE and DFE equalizers, oscillators, and other system components required to represent a serial link.



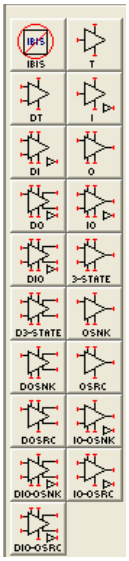
Output Waveform of a DFE shows the convergence and adaptive eye opening



Simulation of a 10 Gbps serial link in ADS.

IBIS Models

IBIS (I/O Buffer Information Specification) is a public-domain, industry-standard specification modeling input and outputs of digital circuits. Digital Semiconductor Vendors may create IBIS models for their parts and distribute them for use in any IBIS-compatible simulator. IBIS simulation provides faster simulation as compared with equivalent-circuit SPICE models. Using IBIS models, the nonlinear effects of integrated circuit I/O buffers can be modeled faster and more precisely, using vendor-supported information. ADS supports most of the IBIS model keywords provided in the IBIS 3.2 specification.

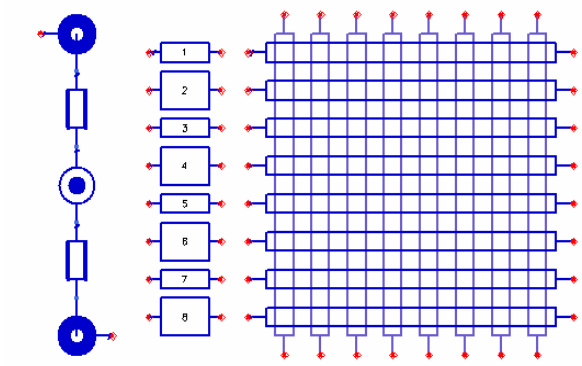


The IBIS model palette.

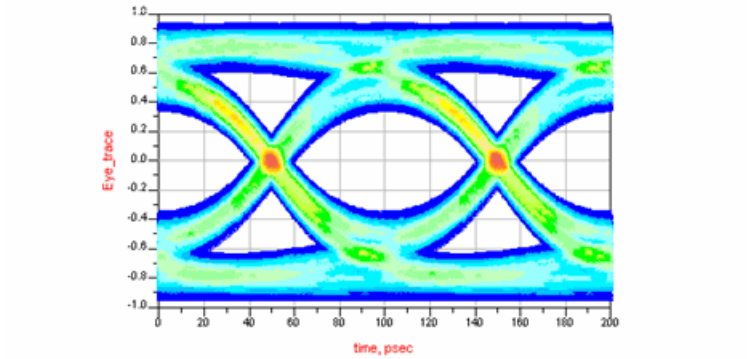
EM-based Multilayer Interconnects Library

This library contains up to 40 metal layers and 80 coupled lines. It improves analysis speed for anticipating layout effects, without requiring the Momentum Planar EM simulator. However, there is a resultant trade off in simulation speed vs. accuracy. The effects of impedance, loss, crosstalk, and delay are modeled with the simplified underlying 2-D electromagnetic field solver associated with these models.

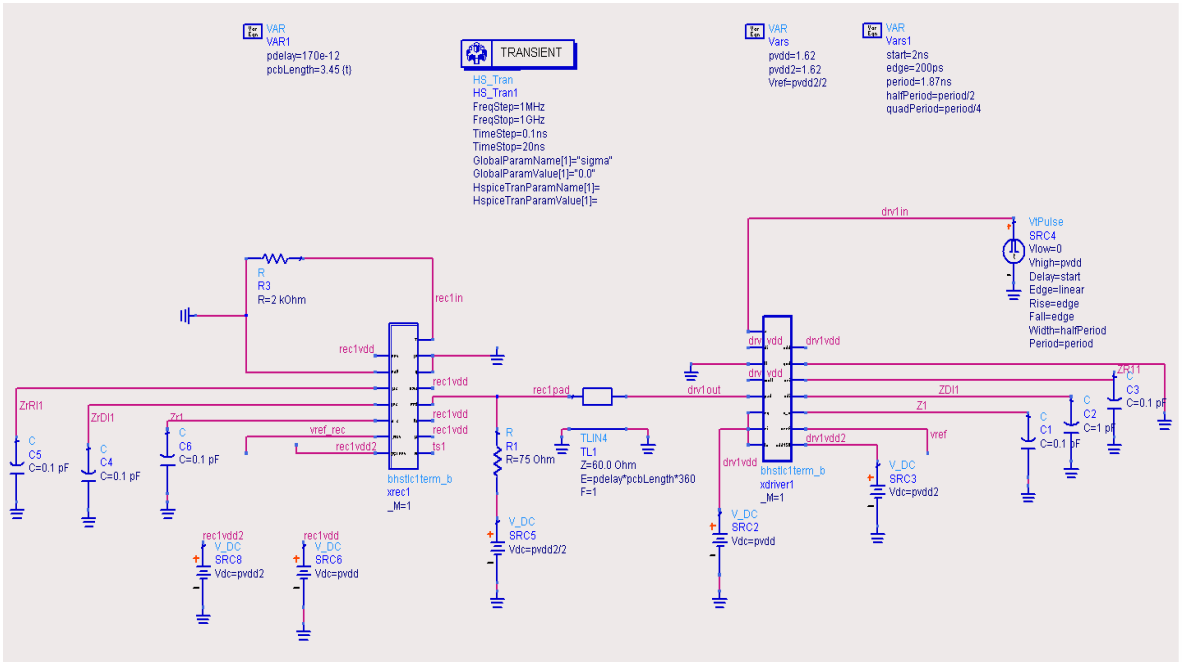
The advantages of the Multilayer Interconnect Models over microstrip and stripline models are that a greater number of coupled line models are available, models can be placed on any specific layer, and you do not need to specify microstrip or stripline operation because it is computed automatically.



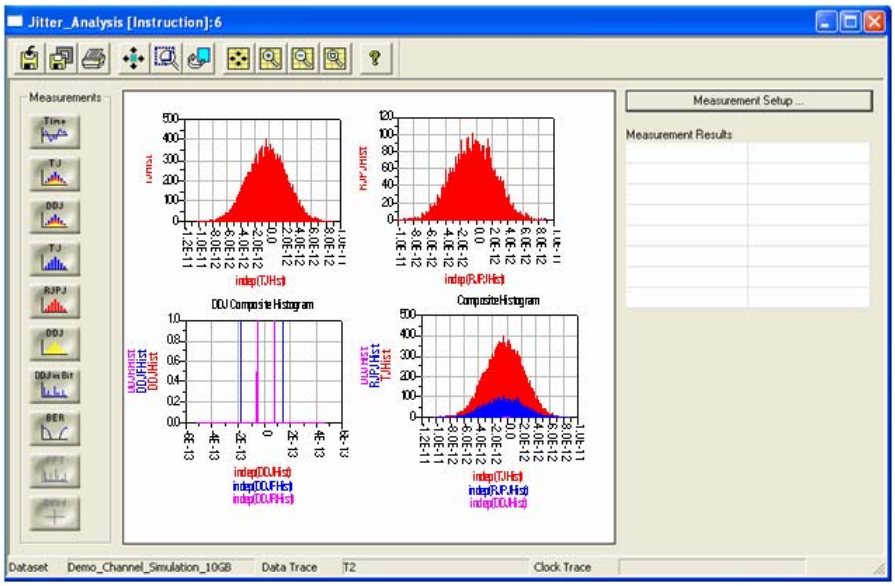
The Eye Diagram front panel allows designers to calculate all the eye diagram parameters using an interface that is similar to that of Agilent instruments.

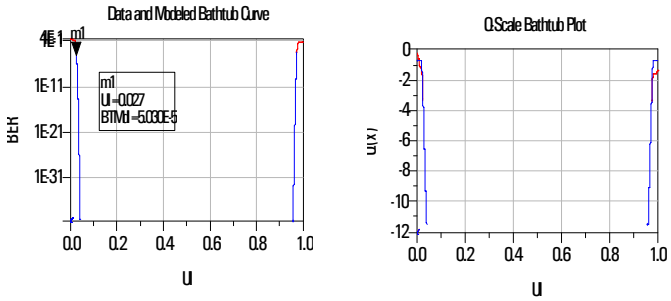


ADS allows easy import of encrypted HSPICE I/O models and simulation using the HSPICE simulator.



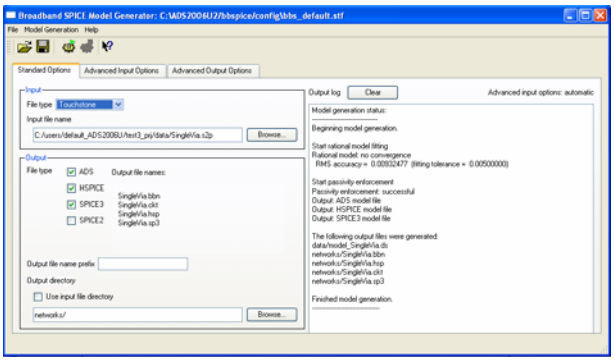
ADS provides powerful jitter analysis for analyzing all the random and deterministic jitter components present in a digital signal. It also provides accurate BER bathtub plots. The capability is based on patented EzJit+ technology, which is available in Agilent's real-time oscilloscopes.

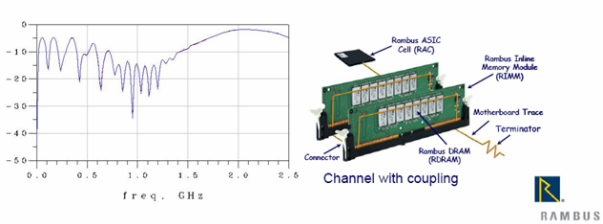




Broadband SPICE Model Generator

Broadband SPICE Model Generator allow designer to import measured or simulated S-parameter data and create SPICE compatible models. Designer can create either Pole-Residue or lumped equivalent circuits. The optional passivity enforcement allow designer to create well behaved models





Comparison of Broadband SPICE model with Original S-parameter for a Rambus™ Device

ADS Signal Integrity Designer bundles come in different configurations to meet your design requirements. The following product configuration matrix illustrates the capabilities in each bundle.

	Signal Integrity Designer	**Signal Integrity Designer Pro**	**Signal Integrity Designer Premier**
Linear Simulator	**X**	**X**	**X**
High Frequency SPICE	**X**	**X**	**X**
Convolution Simulator	**X**	**X**	**X**
IBIS Models	**X**	**X**	**X**
Momentum Simulator		**X**	**X**
Encrypted HSPICE simulator		**X**	**X**
Jitter Analysis		**X**	**X**
Broadband SPICE Model Gen.		**X**	**X**
Ptolemy Simulator			**X**
EMDS for ADS			**X**

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Preliminary Technical Overview

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