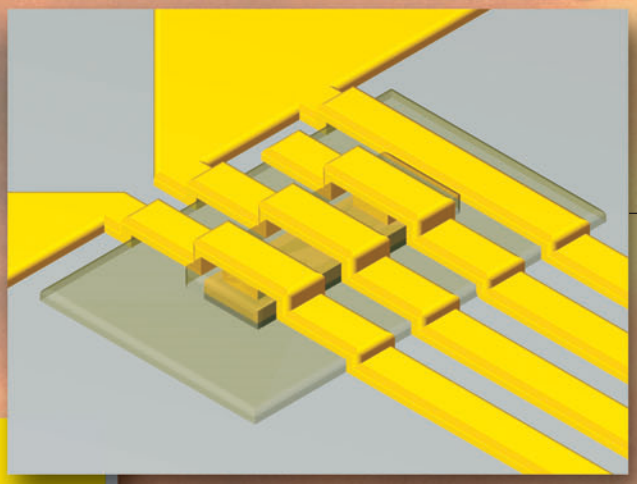
UltraSource

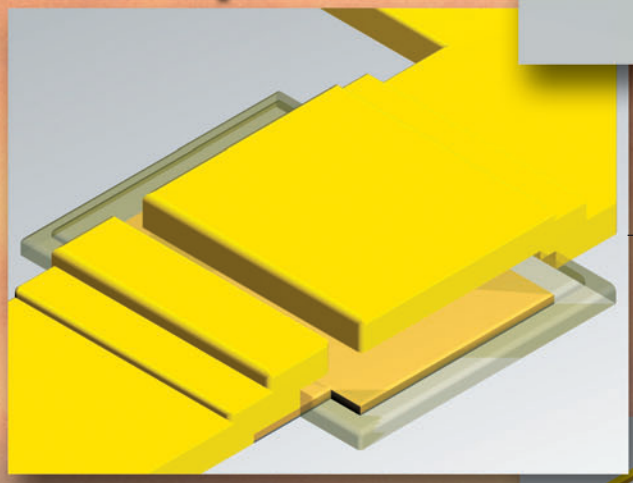
Expanding the frontier of thin film innovation

When you choose UltraSource as your thin film manufacturing partner you get more than a world-class manufacturing facility at your service, you get to take advantage of the latest innovations in thin film today. Innovations that will not only help you solve critical size/performance issues, but will also allow you the freedom to integrate more functionality than you ever thought possible.

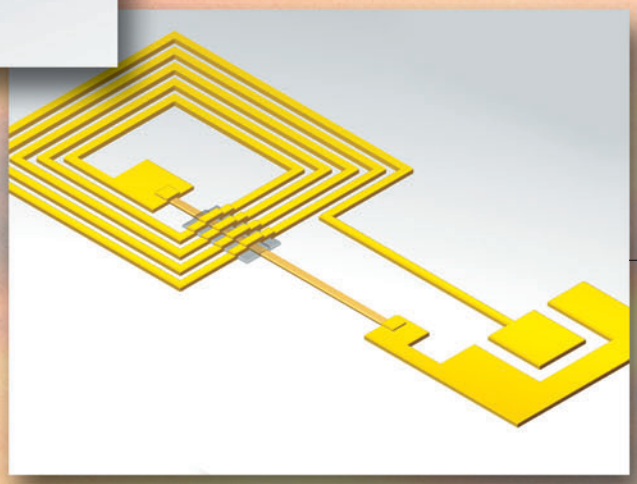
UltraBridge™



UltraCapacitor™



UltraInductor™



UltraBridge is an innovative solution to the inherent problems related to wire bonds and standard air bridges. In this unique process, the interconnect conductor layer is applied and patterned right on the substrate surface. Silicon nitride (Si_3N_4) is then applied as an encapsulation layer and then patterned and etched. Contact windows in the silicon nitride layer are also made. A final standard thin film layer is then applied. The result is a durable, consistent interconnect solution that can be used to replace fragile air bridges. By reducing masks steps and eliminating the need for bond wires, UltraBridge is an extremely cost effective and efficient solution. This approach is available on a custom basis and has also been used in the design and fabrication of a new line of UltraSource Lange Couplers.

UltraCapacitor employs the same technology used in UltraBridge. By employing the silicon nitride as the dielectric layer between the upper and lower electrodes, UltraSource is capable of integrating capacitor elements from 2pF to 250pF directly into thin film circuit designs. Spaces as small as 1 mil (25.4 microns), controlled to tolerances of 2.5 microns, can be achieved. With capacitance designed in, the door is open to a variety of other component integration ideas.

UltraInductor also employs the same technology used in UltraBridge, but creates convenient center tap spiral inductors directly on the substrate. This technique completely eliminates the variability and parasitic problems related to wire bonds. It also insulates one conductor from the other, creating repeatable and consistent inductor connections. The result is a cost efficient solution that offers a tremendous amount of design flexibility.

Our goal at UltraSource is to make the transition from your CAD design to our factory floor as efficient as possible. From our sales and engineering departments, to our dedicated program managers, everyone at UltraSource is here to ensure your devices run smoothly through our process. Since 1991 we've been dedicated to the science of thin film and can help you choose the proper materials for the job and implement the latest technologies and design approaches.

Tap into our focused facility and vast experience
When your circuit challenges require professional expertise to solve critical issues, you need a supplier that has overcome a variety of issues in various markets. In addition to being focused on becoming the most efficient end-to-end thin film manufacturing facility in the business, we've also made it a point to find a balance in the markets we serve. As a result, we've experienced nearly every thin film design/manufacturing challenge imaginable, and can put that experience to work for you.

Markets we serve:
- Defense and Homeland Security
- Telecommunications
- Sensors
- Medical Imaging
- Biotech/Microfluidics

Device types and interconnects we manufacture (singular or integrated):
- Broadband and narrowband RF/Microwave circuits
  - Lange Couplers
  - Power Dividers
  - Filters
  - Delay Lines
  - Circulators
  - Isolators
  - Resistors
  - Attenuators
  - Ferrites
- Integrated multilayer interconnects with
  - UltraBridges
  - UltraInductors
  - UltraCapacitors
- Infra-red windows
- Laser diode submounts
- Lab-on-a-chip circuits

Our quality is second-to-none
In a world of customization and technical challenges, we understand the importance of customer service, communication, and process control. From the moment you request a quotation, to the moment your product is shipped, we strive to let you know we're on top of the details. And nothing is more important to us than delivering circuits just the way you want them, right when you need them.

Our quality assurance system is based on MIL-I-45208A, MIL-Q-9858, and ISO 9001. Our products are 100% visually inspected to meet and exceed customer and MIL-STD-883 (method 2032) requirements.

Our QA system includes:
- Quality Assurance Manual (revision controlled)
- Documented QA and Manufacturing Procedures (revision controlled)
- 100% inspection of all critical incoming materials
- Equipment maintenance meets MIL-C-45662 with monthly and annual calibrations
- Sputter lot coupons maintained on file for three years
- Testing available per MIL-STD-883 or MIL-PRF-38534
- 100% inspection of each order to meet/exceed MIL-STD-883 (method 2032) as well as customer specified requirements
- First article inspection reports available upon request

CAPABILITIES AND EXPERTISE

From prototypes to high volume manufacturing
UltraSource's staff and facilities are ready to assist you with everything from your first prototype to a million units.

Dedicated program management
From product managers to applications engineering and project management, UltraSource provides you with a cohesive support team.

Your choice of substrates
UltraSource is an expert at working with the following substrates: alumina, fused silica, aluminum nitride, beryllium oxide, ferrite, PZT, titanates, glass, quartz, sapphire, garnet, and silicon.

Polymide films
UltraSource offers the option of patterned polyimide films for use as a solder mask, via fill and insulating layer.

Sputtering capabilities
UltraSource guarantees superior thin film bonding characteristics for various metal systems, starting with the industry standards of titanium-tungsten, nickel (optional), and gold for all substrate materials. You also have the option of the following metals deposited using sputtered and/or electroplating: copper, silver, palladium, platinum, aluminum, chrome, titanium, and molybdenum.

Filled vias and plated through-holes
Solid filled vias are available in gold, silver, tungsten, and copper-tungsten. (Slots are also available.) Plated through-holes have diameters as low as 50% of the substrate thickness. Edge wrap-around techniques, including patterned edge wraps, can connect isolated front-to-back conductors.

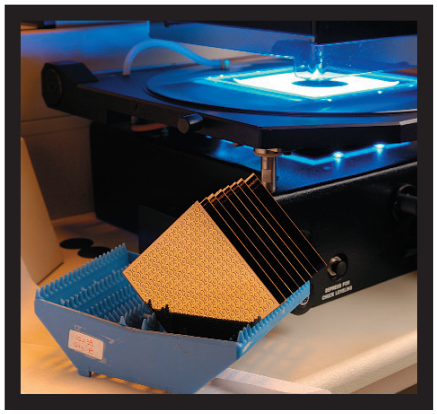
Resistor films
Resistors are a logical extension to thin film circuit designs and are easily integrated with circuitry using Tantalum Nitride or NiChrome films that are available for many applications and ranges. A wide variety of sheet resistivities is available for all high-value, close-tolerance, and tight space requirements.

Pre-deposit patterned solder
AuSn pre-deposited solder eliminates the need for pre-forms and improves assembly efficiency and reliability. Additionally, this option can be configured for feature sizes as small as .002" square. Pre-deposited AuSn thickness range is from 3 to 10 µm.

Photolithography and etching of patterns
UltraSource incorporates the use of both Mylar and glass photo masks for use in our photolithography processes. We can routinely achieve accurate patterning of feature sizes down to .001" (25.4 µm). On a custom basis, .0004" (10 µm) can be achieved. Standard patterning tolerances are ± .0002" (5 µm) with special tolerances from ± .0001" (2.5 µm) down to ± .00005" (1.25 µm).

Singulation
Singulation of thin film circuits from the substrates is achieved using the latest in high speed dicing saws and diamond based blades. This technology offers the most efficient means of singulating a broad range of substrate materials and metals The standard tolerance is ± .001" (25.4 µm) and special tolerances of down to ± .0005" (12.7 µm) are available.

Multilayer solutions
By combining our extensive knowledge of various substrates with our advanced UltraBridge, UltraInductor, and UltraCapacitor technologies, we can offer you multilayer solutions to circuit challenges that you might never have thought possible.



Use this thin film design guide to help you design the best circuit for the job

We've assembled this design guide to help you with some of the critical decisions of your circuit design. Use it to choose the proper substrate material for a high power circuit, or the right conductor or resistor film that will help you avoid wire bonding problems. If you're considering an integrated resistor, see page 8 for a brief overview on how to properly design resistor length and width to gain your desired resistivity. And if you're considering plated through-holes or vias see page 9, where we review the proper hole dimensions and annular borders for through-holes, and the material options and design considerations for solid filled vias.

We've also included notes on how to best prepare your CAD files so they interface with our program management team seamlessly. Plus, you'll find design parameters for our innovative Ultra- technologies, so you can begin designing these innovations into your circuits right away.

For additional assistance, please give our application engineering department a call at 800-742-9410

Commonly Used Conductor/Resistor Films

Metallization	**WTi/Au**	**WTi/Ni/Au**	**WTi/Cu/Ni/Au**
Typical Applications	• Devices processed at high temperatures, such as Au/Ge eutectic bonding temps	• Devices processed at higher temperatures requiring a solderable film	• High conductivity film allowing for wire bonding and/or soldering after high temp. processing
Advantages	• Film withstands excursions to 450°C	• Film withstands brief excursions to 325°C	• High conductivity film • Pb/Sn & Au/Sn solderable
Disadvantages	• Not Pb/Sn, Au/Sn Solderable	• Wire bonding problems may be possible due to Ni-Au diffusion when devices processed > 300°C	• Wire bonding problems may be possible due to Ni-Au diffusion when devices processed > 300°C
Temperature Guidelines	• 450°C for 30 minutes	• 300°C for 120 minutes	• 300°C for 120 minutes
Pb/Sn, Au/Sn Solderability	• Poor	•Good	• Good
Allowable Die Attach Methods	• Epoxies • Au/Ge eutectic • Au/Si eutectic • Au/Sn eutectic • Pb/In eutectic	• Pb/Sn solder • Au/Sn solder • Epoxies • Pb/In eutectic	• Pb/Sn solder • Au/Sn solder • Epoxies • Pb/In eutectic
Typical TCR	n/a	n/a	n/a
Front Side Metal	• Sputtered WTi 300-500Å • Sputtered Au 20-300µ"	• Sputtered WTi 300-500Å • Sputtered Ni 2,000-5,000Å • Sputtered Au 20-300µ"	• Sputtered WTi 300-500Å • Sputtered Cu 40µ" • Electroplated Cu 40-2000µ" • Electroplated Ni 50-150µ" • Electroplated Au 50-250µ"
Back Side Metal	• Same as front side	• Same as front side	• Same as front side

Note: The information supplied in this brochure is offered as an assistance to engineers and buying agents. UltraSource makes no certification as to the suitability of material for any application.

Substrate Material Properties

Material	CLA Surface Roughness (µ-inches)	Thickness Available (inches)	Dissipation Factor at 1 MHz	Dielectric Constant (k)	Thermal Conductivity (W/mK)	Coefficient of Thermal Exp. (ppm/°C)	Applications
As fired/Lapped or Polished 96% Alumina	≤ 35	.010–.250	0.0004	9.5	26	6.3–8.0 (25–1000°C)	Low to medium power DC & RF circuits
As fired 99.6% Alumina	< 4	.005–.040	0.0001	9.9	30	7.0–8.3 (25–1000°C)	Low to medium power DC & RF circuits
Polished 99.6% Alumina	< 2	.004–.040	0.0001	9.9	30	7.0–8.3 (25–1000°C)	Low to medium power RF and microwave circuits
Lapped Aluminum Nitride	25	.004–.120	0.001	8.6	170 min.	4.6 at (25 – 300°C)	High power DC/RF/ microwave circuits
Polished Aluminum Nitride	< 3	.004–.080	0.0005	8.6	170 min.	4.6 (25 – 300°C)	High power DC/RF/ microwave circuits
Polished 99.5% Beryllium-Oxide	< 3	.007–.080	0.0004	6.5	250 min.	6.4–8.6 (25–1000°C)	High power DC/RF/ microwave circuits
Borosilicate Glass	< .5	.030–.200	n/a	4.6 (at 1 MHz and 25°C)	1.12	3.25 (25 – 300°C)	biomedical
Sapphire	< .1	.003–.250	0.00086/ 0.0003	9.3–11.4	40	A plane at 25°C 5.3	Optical
Polished Fused Silica	< .1	.003–.040	0.000015	3.8	1.4	0.56	High frequency circuits requiring extremely low loss performance
Polished Titanates	< 3	.005–.080	0.0004	38 - 200	1.8–4.2	5.8	RF & microwave circuits requiring high Q

	TaN/WTi/Au	TaN/WTi/Ni/Au	NiCr/Ni/Au
	• Devices processed at high temperatures, such as Au/Ge eutectic bonding temps	• Devices processed at higher temperatures requiring a solderable film	• Designs requiring precision resistors with low TCR's
	• Film withstands excursions to 450°C • Passivated TaN films offer good humidity resistance	• Pb/Sn & Au/Sn solderable • Passivated TaN films offer good humidity resistance	• Low TCR's (0 ± 50 ppm/°C) • Pb/Sn & Au/Sn solderable
	• Not Pb/Sn or Au/Sn Solderable • Should be fully sputtered in order to provide blister free films	• Wire bonding problems may be possible due to Ni-Au diffusion when devices processed > 300°C	• Wire bonding problems may be possible due to Ni-Au diffusion when devices processed > 300°C
	• Stabilize resistors at 425°C for 30–120 minutes	• Stabilize resistors at 325°C for 60 minutes	• Stabilize resistors at 325°C for 60 minutes
	• Poor	• Good	• Good
	• Epoxies • Au/Ge eutectic • Au/Si eutectic • Au/Sn eutectic • Pb/In eutectic	• Pb/Sn solder • Au/Sn solder • Epoxies • Pb/In eutectic	• Pb/Sn solder • Au/Sn solder • Epoxies • Pb/In eutectic
	• -100 ± 50 ppm/°C	• -100 ± 50 ppm/°C	• 0 ± 50 ppm/°C
	• Sputter 10-200 Ω/sq. TaN • Sputtered WTi 300-500Å • Sputtered Au 20-300µ"	• Sputter 10-200 Ω/sq. TaN • Sputtered WTi 300-500Å • Sputtered Ni 2,000-5,000Å • Sputtered Au 20-300µ"	• Sputter 50-200 Ω/sq. NiCr • Sputtered Ni 2,000-5,000Å • Sputtered Au 20-300µ"
	• Same as front side without the TaN layer	• Same as front side without the TaN layer	• Same as front side (NiCr for adhesion only)

Integrated current regulation, power termination, and voltage division using thin film resistors
Resistors are a logical extension to thin film circuit designs. They are easily manufactured with all other circuitry using Tantalum Nitride or NiChrome films, and provide efficiently integrated current regulation, power termination, and voltage division.

UltraSource offers a wide variety of sheet resistivities (see pages 6–7) for all your high-value, close-tolerance, and tight-space requirements. Standard values from 1ohm to 1,000 ohms can be achieved. Standard tolerance for all resistor values are ± 10%, and custom tolerances as low as ± .5% can be achieved using our laser trim process.

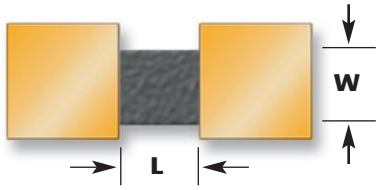
Understanding thin film resistor fabrication
A basic understanding of thin film resistor fabrication can assist you in your circuit design. Thin film resistors are fabricated by sputtering a high-resistance film of Tantalum-Nitride (TaN) or NiChrome (NiCr) under the conductor layer and selectively etching the resistor elements. The following table shows how typical characteristics of Tantalum-Nitride (TaN) and Nichrome (NiCr) films can be used to obtain desired performance.

Film Type	Sheet Resistivity (ohm/square)	TCR (ppm/°C)	Passivated Tolerances (no trim)	Laser Trimmed Tolerances
TaN	10–200	-100 ± 50	± 10%	± 0.5–10%
NiCr	50–225	0 ± 50	± 10%	± 0.5–10%

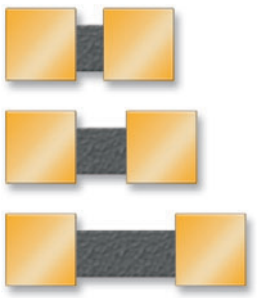
Once you have selected a resistor film type and desired resistivity, the elements are designed under the following rules:

R = p(L/W)

R = total resistance of the elements (ohms)
P = sheet resistivity (ohms/square)
L= resistor length (distance between the conductors)
W = resistor width (width of the resistor element)



This formula demonstrates that the aspect ratio of L/W becomes a simple means of designing for the total resistance of the element. Examples of resistor elements, using a 50 ohm/square film, are demonstrated here:



L = .5W
L/W = .5
R = 25 ohms

L = W
L/W = 1.0
R = 50 ohms

L = 2W
L/W = 2.0
R = 100 ohms

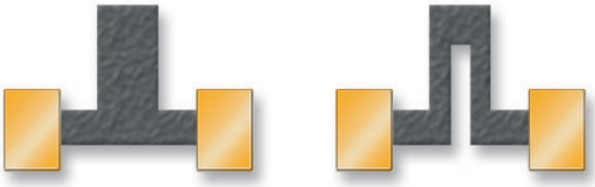
Choose from three primary types of thin film resistor layouts
Block elements, meander resistors and top hat elements are the three primary types of thin film resistor layouts.

Block elements are used as a low value resistor element

Meander resistors are used as a high value resistor element, but in series with a top hat element that provides a reliable laser trim.

Note: when calculating the L/W of the total element, each right angle turn adds 0.5 to the total.

Top hat elements are used as a high value laser-trimmable resistor element

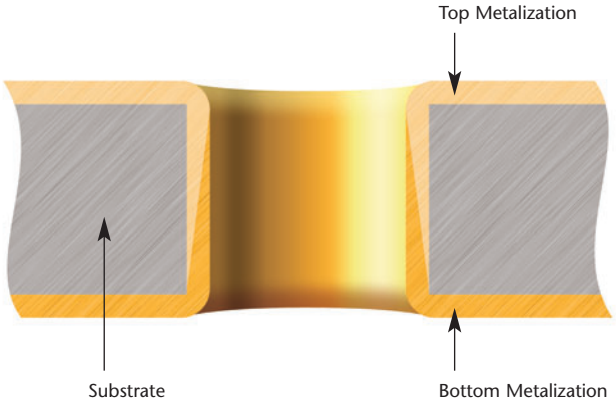


Design considerations for laser trimmed vs. non laser trimmed circuits
Thin Film Resistor elements should be designed at either 80% or 100% of final value according to the following guidelines:

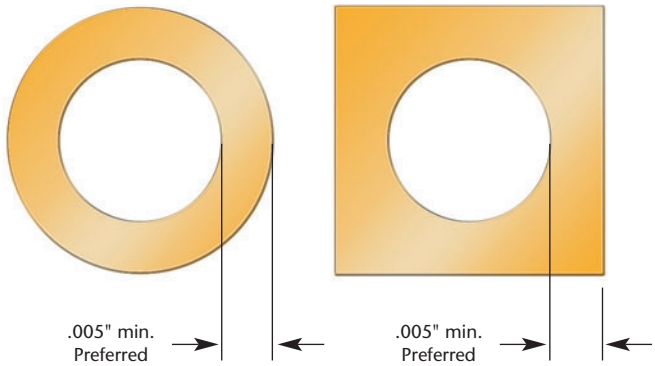
Resistors with no laser trim should be designed at 100% of final value. Non-laser trimmed resistors are used to reduce cost and lead-time and provide a resistor value tolerance control of ±10% or greater.

Resistors with laser trim (tolerances < ± 10%) should be designed at 80% of final value to allow for laser up-trimming.

Your choice of plated through-holes or filled vias
UltraSource offers two options for pass-through conductance. First, we offer highly reliable plated through-holes, with diameters as low as 50% of the substrate thickness. These through-holes are laser drilled, de-slagged and repetitively cleaned for optimum metallization adhesion, and they are sputtered from each substrate side for maximum step coverage and reliability. When necessary, edge wrap around techniques, including patterned edge wraps, can connect isolated front-to-back conductors.



Annular borders around plated through-holes:



Plated through-hole sizes:

Substrate Thickness	Preferred Hole Diameter	Allowable Hole Diameter
.005	ø.004"	ø.003"–.005
.010	ø.006"	ø.006"–.010
.015	ø.008"	ø.008"–.015
.020	ø.010"	ø.010"–.020
.025	ø.012"	ø.012"–.025

To address issues that are sometimes associated with plated through-hole technology, UltraSource also offers solid filled vias. These vias eliminate epoxy and/or solder extrusion during assembly process, provide a planar and low-resistance microwave grounding path, and offer a high thermal conductivity cooling path for high power die.

UltraSource offers three types of solid filled via circuits. They are available on alumina (Al_2O_3), aluminum nitride (AlN) and beryllium oxide (BeO) substrates and are post polished to provide a high quality, planar surface.

- **Solid gold (Au) filled vias**
- **Solid silver (Ag) filled vias**
- **Solid copper-tungsten (CuW) filled vias**

Solid filled via design parameters:

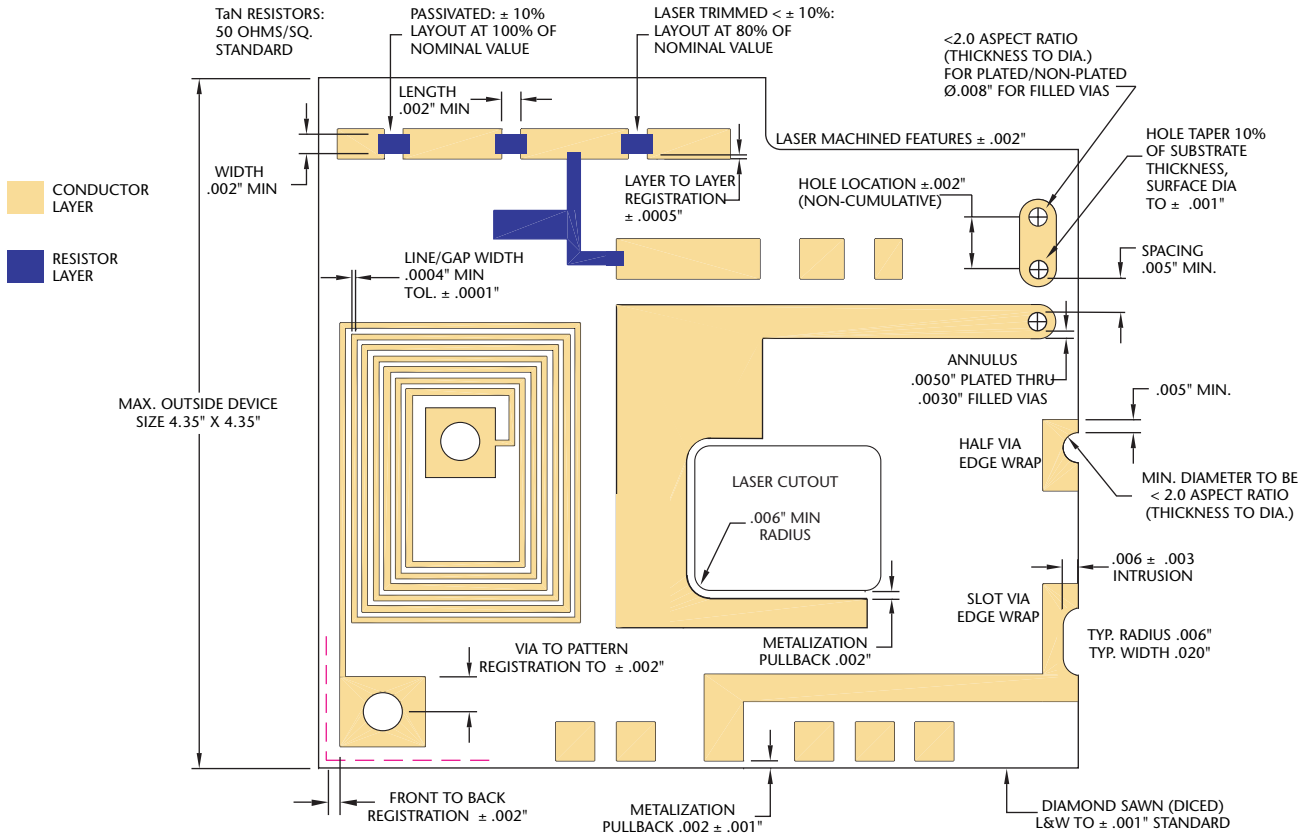
Substrate Thickness	Filled Via Diameter	Substrate Materials	Center to Center Spacing
.005"	ø.005"	Al_2O_3, AlN, BeO	.012"
.010"	ø.008"	Al_2O_3, AlN, BeO	.025"
.015"	ø.008"	Al_2O_3, AlN, BeO	.027"
.020"	ø.010"	Al_2O_3, AlN, BeO	.029"
.025"	ø.012"	Al_2O_3, AlN, BeO	.031"

Requirements for designing UltraBridge, UltraInductor, and UltraCapacitor circuits

Parameter	UltraBridge/UltraInductor Requirement	UltraCapacitor Requirement	Units
Base Conductor	WTi/Au	WTi/Au	N/A
Base Conductor Thickness	5,000 to 15,000	0.5x dielectric thickness (max)	Å
Minimum Line (Base)	0.4 (10)	N/A	mil (µm)
Minimum Gap (Base)	0.4 (10)	N/A	mil (µm)
Dielectric	Si_3N_4	Si_3N_4	N/A
Dielectric Constant	7.8	7.8	N/A
Dielectric Thickness	~10,000 to ~30,000	~5,000 to ~10,000	Å
Capacitance Density	N/A	0.05 to 0.10	pF/mil2
Dielectric Overlap of Base Conductor	1.0 (25) min.	1.0 (25) min.	mil (µm)
Dielectric Vias	1.0 (25) min.	N/A	mil (µm)
Dielectric Pads	3.0 (75) min.	N/A	mil (µm)
Top Conductor	To design	To design	N/A
Top Conductor Thickness	2x dielectric thickness (min)	2x dielectric thickness (min)	N/A
Capacitor Value Range	N/A	2–250	pF
Capacitor Tolerance	N/A	±10 (≤50 pf) / ±20 (>50 pf)	%
Capacitor Around Via	N/A	Acceptable*	N/A
Minimum Line (Top Conductor)	1.0 (25)	N/A	mil (µm)
Minimum Gap (Top Conductor)	0.5 (12)	N/A	mil (µm)
Material	99.6% Al_2O_3 & AlN*	99.6% Al_2O_3 / AlN*	N/A
Substrate Surface Finish	Polished	Polished	N/A

* Subject to Engineering Review
mil = 0.001" = .025mm = 25.4µm

Guidelines for thin film layout and design



Preparing your CAD files for successful thin film circuit production

UltraSource has a talented team of CAD professionals to convert your CAD designs from source control drawings into the various documents needed for thin film processing. To facilitate these documents, we request that you incorporate the following information and design guidelines in your CAD package so that we may accurately process your design(s).

CAD requirements:

1. File format must be in AutoCAD .dxf or AutoCAD .dwg file extensions. Gerber or .gbr files are not preferred, as translation errors may occur in converting to the appropriate format.
2. Zero width polylines are needed to create closed boundary polygons for all geometries.

YES NO

3. Avoid double entities or extraneous lines, as this will lead to uncertain interpretation the CAD design and will delay lead times.

YES NO

4. All drawings must be drawn in a two dimensional (2D) format.
5. Each design feature should be drawn on separate layers as shown below:

CAD Layers
1. Device (substrate) Outline
2. Conductor Layer, Shaded, Front and/or Back
3. Dimensional Layer
4. Resistors (if required)
5. Via, Plated Through-Holes (if required)
6. AnSn Layer (if required)
7. Dielectric, Solder Dam (if required)
8. Other Layers That May Exist (if required)

6. In order to avoid polarity confusion, metallized areas should be shaded or cross-hatched to indicate where metal is desired.
7. Data or features that are not part of the thin film design should be placed on a separate, reference only layer.
8. Units shall be listed in either Imperial (English) or Metric units. Dimensions to be identified as inches, millimeters or microns. At least one overall dimension is required on the substrate layer if part needs to be scaled to size.
9. A critical dimension for each layer should be supplied, with a tolerance, on the dimensional layer.

SCD requirements:

1. Metal layers must include the following details by order. Thickness and tolerance must be listed:

Resistor Layer	50Ω/sq. TaN, TCR -100±50ppm/°C
Conductor Layer Tungsten-Titanium (WTi): Nickel (Ni): Gold (Au):	 500Å ± 100 2,000Å ± 500 100µ" ± 25µ"
Solder Layer	4±1µm Pre-deposited 73/27 AuSn
Ground Plane Tungsten-Titanium (WTi) Gold (Au):	 500Å ± 100 100µ" ± 25µ"

2. Substrate thickness, tolerance and finish must be identified:

Alumina, as-fired	99.6%
Thickness	0.025"±0.002"
Surface Finish	<4µ" CLA
Camber	0.001"/"

3. Specialty inspection requirements should be listed (i.e. bake testing, TCR).
4. Customer name, customer part number and revision level must be listed on SCD.
5. Resistance and/or capacitance charts should be provided:

Resistor	Nominal (Ω)	TOL	Length	Width
R1, R4	18.8	+5/-20%	.0150	.0400
R2, R5	15	+5/-20%	.0150	.0500
R3, R6	12.5	+5/-20%	.0150	.0600
R7, R10	16.5	+5/-20%	.0150	.0450
R8, R11	25	+5/-20%	.0150	.0300
R9, R12	50	+5/-20%	.0150	.0150
R13, R16	50	+5/-20%	.0450	.0450
R14, R17	16.5	+5/-20%	.0150	.0450
R15, R18	11	+5/-20%	.0100	.0450
R19, R22	25	+5/-20%	.0200	.0400
R20, R21	12.5	+5/-20%	.0100	.0400

6. Additional layers thickness and tolerance must be called out (i.e. SiN, polyimide).

Dielectric layer	20,000Å ± 5,000Å Si_3N_4

7. Additional layer properties must also be called out (i.e. 80/20 Au/Sn versus 70/30 Au/Sn).

Solder layer	4±1µm Pre-deposited over 73/27 AuSn

8. All pullbacks should be identified and dimensioned.
9. Plating requirements must be defined.
10. Front to back registration tolerance should be listed when applicable.
11. Camber requirements should be listed.
12. Filled vias must specify material Eg: Gold, Copper Tungsten, etc.
13. Plated through-hole and via locations, diameters, and tolerances should be dimensioned.

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