Implications of Using kW-level GaN Transistors in Radar and Avionic Systems

Daniel Koyama, Apet Barsegyan, John Walker

Integra Technologies, Inc., El Segundo, CA 90245, USA

Abstract **This paper examines the effect of using normal Class A/B bias for kW-level GaN and LDMOS transistors used in radar and avionic systems. It is shown that Class A/B bias results in an overall efficiency which is typically 5-10% less than the efficiency during the pulse as well as generating significant shot noise in the off period which can cause receiver de-sensitization. A novel automatic gate pulsing and sequencing circuit is described which overcomes both of the above problems. Rise/fall time and latency measurements are presented for this circuit. It is shown that the output noise in the off period is reduced by >30dB.**

Index Terms **— GaN, Transistors, radar, avionics.**

I. Introduction

Pulsed Silicon bipolar transistors with power outputs exceeding 1kW for use at GHz frequencies have been available for a few decades. Bipolar transistors are very well-suited to this application, and the technology is very mature and extremely reliable. Bipolar transistors offer a number of advantages over LDMOS and GaN HEMTs for this application including the ability to operate from just a single positive supply voltage, they have the simplest and cheapest circuits of any technology, and the ability to operate in class C which means that negligible shot noise is injected into the receiver in the pulse off-period, and there is no efficiency degradation due to power being consumed by the quiescent current in the pulse off period. However, bipolar transistors also have a few disadvantages, for example they require the use of environmentally unfriendly BeO packages, which is a major cost-driver, and they have low gain, typically around 9dB for a 1kW device compared with 18-20dB for a typical GaN or LDMOS part. The low gain means that more driver stages are required which adds to both cost and size of the amplifier as well as degrading the overall efficiency.

LDMOS devices with a power output of a kW have been available for about 10 years. Early devices were prone to failure due to latch-up of the inherent parasitic bipolar transistor in the device. This happens because pulsing of the device results in a very large change in drain current in a short period of time, and since this current passes through an inductor in the drain bias circuit then a spike voltage appears across the drain of the transistor through *Ldi/dt* action. This spike can trigger latch-up of the parasitic bipolar transistor leading to device failure. The higher the power of the transistor, the higher the current which leads to a higher spike voltage which makes kW-level LDMOS devices more susceptible to this type of failure mode. Although today's LDMOS transistors are much more robust than the early ones in withstanding this spike voltage, failures can still occur. Nevertheless, kW-level LDMOS transistors are available from a number of manufacturers for avionics applications including IFF, SSR, and TACAN/DME as well as L band radar. LDMOS transistors have much higher gain of around 18-20dB compared with 9dB for a bipolar. They also do not need BeO packages, both of which result in a significant cost reduction. However, LDMOS has about 5-10% less efficiency than a bipolar transistor since the former are always operated in Class A/B whereas bipolar transistors are operated in Class C.

Within the last few months kW-level GaN transistors have been released [1,2] for avionic and L band radar applications. These devices offer similar gain to LDMOS and have a comparable price, but they have the highest efficiency of any of the three technologies at about 80%. The higher efficiency is a consequence of various factors including having a lower on-resistance due to the very high mobility of the 2D electron gas within the HEMT epi-layer, and the ability to present optimized impedances at the harmonics due to the much lower capacitance. The lower capacitance also results in a higher transistor output impedance which requires a lower impedance transformation ratio in the output matching network which thus has less loss.

While GaN and LDMOS transistors have significant advantages compared with bipolar transistors for avionic and radar applications, they both have one very significant disadvantage, namely they are both biased in Class A/B which means that the transistor will have a quiescent current flowing through the device in the pulse-off period. Quiescent current is roughly proportional to output power so this power dissipation becomes a significant issue for kW-level transistors. Avionic and radar applications typically use a 10% duty cycle so this means that the transistor is consuming its quiescent current for 90% of the time. Figure 1 shows the effect of this quiescent current on the overall efficiency of a 1kW GaN transistor for IFF/SSR applications. The efficiency during the pulse is 81.5% but the overall efficiency is reduced to 75.2% after allowance is made for the quiescent current consumed in the pulse off period.

There is another serious issue with using GaN or LDMOS, namely the quiescent current in the pulse-off period generates shot noise [3] given by

$$I_n^2 = 2qI_{dq}B \qquad (1)$$

where I_n^2 is the rms noise current, q the electron charge, I_{dq} the quiescent current and B the bandwidth. This shot noise can enter the receiver causing receiver de-sensitization.

A final disadvantage of GaN is that it is a depletion-mode device which means that it needs both positive and

negative supply voltages, and the drain voltage needs to be applied after the gate voltage is set to the required value to prevent excessive current from flowing causing device destruction.

To avoid the efficiency degradation and eliminate receiver desensitization it is essential that the quiescent current is reduced to zero in the pulse-off period. This can be done by pulsing either the gate or drain voltage in synchronization with the RF pulse. Gate pulsing is simpler to implement since for a kW-level transistor drain pulsing would require switching around 20A, but the transistor will still consume a small amount of current in the pulse-off period determined by its leakage current which may be a few mA, whereas drain pulsing reduces this current to almost zero. This paper will report on a novel pulsing scheme for GaN transistors that also eliminates the need for a negative supply voltage, is fully automatic in that it is triggered by the application of an RF pulse to the transistor, and provides fail-safe biasing of the transistor by ensuring the correct sequencing of gate and drain voltages. Rise and fall time measurements will be presented along with pulse latency and noise output improvement. Temperature compensation will also be discussed.

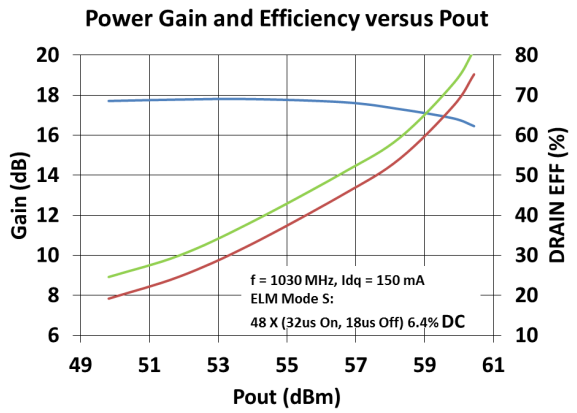


Fig. 1. Effect of quiescent current in the off period on overall efficiency. Red curve is overall efficiency, green curve efficiency during the pulse, blue curve is associated gain.

II. GATE PULSING AND SEQUENCING CIRCUIT

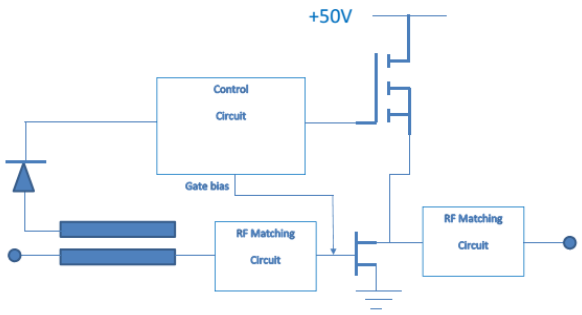


Fig. 2. Block diagram of Gate Pulsing and Sequencing Circuit.

Figure 2 shows a block diagram of the pulsing circuit while Figure 3 shows the circuit in complete detail. A detector is used to sense when an RF signal is applied to the transistor. The MOSFET in series with the GaN device is initially turned off, the voltage applied to the gate of the GaN device is then set to the required value to achieve the desired quiescent current, and then the MOSFET is turned on. Once the correct gate bias is applied to the GaN device, all subsequent switching of this device is accomplished through gate pulsing alone. This circuit has several advantages:

1). Only a single positive supply voltage is needed, all other voltages are generated in the control circuit.

2). It is fail-safe in that the circuit automatically ensures that the gate voltage is negative before drain bias is applied to the GaN device, thereby preventing accidental device destruction.

3). The voltage drop across the ultra-low R_{dson} MOSFET is typically 0.2V which means that the efficiency during the pulse is degraded by only about 0.3%.

The detailed operation of this circuit is as follows:

At initial DC power-up, Q4 remains off while the +5V voltage regulator U2 and voltage inverter U3 turn on. The output of U2 drives the input of U3 to produce the -5V needed for the GaN transistor gate biasing. When the positive supply voltage reaches about +4 volts, U3 begins to turn on and negative voltage appears at its output. When U3 output voltage reaches about -4 volts, NPN transistor Q3 turns on, which turns on the P-channel MOSFET Q1. With Q1 on, its source terminal goes to 0V, turning off the N-channel MOSFET Q2. The open-circuit at the drain of Q2 disconnects it from the UV pin (pin1) of U1 and allows normal operation of the controller U1 to proceed. Whenever U3 is off or not fully on i.e., when its output is -4V or less then Q2 will be on, pulling the UV pin of the controller U1 down to 0V and forcing U1 to turn off Q4. This ensures that no drain voltage is applied to the GaN device when the voltage inverter output is not at least < -4V, and that the GaN device will always be pinched off initially when drain voltage is being applied to it.

As power-up proceeds, U1 becomes active and assumes control of the remaining bias sequencing process. When the UV pin of U1 reaches the low-to-high threshold voltage of 4V, the GATE pin (pin 6) of U1 begins to turn on Q4, allowing drain voltage to be applied to the GaN device. The supply voltage at which this occurs can be set by resistors R4 and R5. As an example, for R4=68KΩ and R5=10KΩ, the supply voltage will begin to turn the drain on when it reaches 31V (31*10K/[10K+68K] = 4). The GATE pin of U1 utilizes a charge pump to provide a linear ramp-up of the drain voltage. This ramp-up time can be adjusted with capacitor C5.

For power-down, the process occurs in reverse except that the threshold level is slightly offset due to the built-in hysteresis in controller U1 (high-to-low threshold, pin UV = 3.6V). For the example given above, the high-to-low threshold will be triggered when the supply voltage crosses 28V (28*10K/[10K+68K]=3.6) at which time Q4 turns off.

As described earlier, the negative voltage will not begin to shut down until the supply voltage has dropped below about +4V.

The gate pulsing circuit is DC-powered from the -5V output of the voltage inverter U3, but otherwise operates separately from the bias sequencer. In the off period of the RF pulse, the gate pulsing circuit is inactive and passes the -5V to the gate of the GaN transistor keeping it pinched off. In the pulse-on period, a Schottky diode detector circuit triggers a comparator/switch circuit which switches the gate voltage to the desired operating bias level. The bias can be set in a voltage divider circuit formed by an adjustable potentiometer. For fast switching time, a high-speed rail-to-rail op-amp was used in the buffer amplifier. Also, capacitance on the gate bias line following the switch was minimized to maintain fast rise/fall time.

The total power consumption of this gate pulsing and sequencing circuit is 0.85W (17mA at 50V).

III. MEASUREMENTS

The pulsed voltage waveform applied to the gate is shown in Figure 4, while Figure 5 shows the RF output pulse waveform from which it can be seen that the rise and fall times are 100ns and 16 ns, respectively. For comparison, the rise and fall times for the same transistor with normal gate biasing (i.e. no gate pulsing and sequencing) are 59ns and 15ns, respectively. It is obvious that there must be a delay between the application of the RF pulse and the pulse at the load, this delay is typically 10ns.

Of critical importance is the determination of the output noise improvement in the pulse-off period as a result of using the gate pulsing and sequencing circuit. This data is given in Table 1 from which it can be seen that >30dB suppression was achieved. This data was obtained on a 500W transistor that used 200mA quiescent current in normal operation.

Frequency (GHz)	Input Noise (dBm/Hz)	Output Noise Normal Gate Bias (dBm/Hz)	Output Noise Gate Pulsing (dBm/Hz)
1.2	-126	-113	-147
1.3	-126	-113	-147
1.4	-126	-113	-148

Table 1: Amplifier noise power: normal gate bias vs. gate pulsing for I_{dq}=200mA.

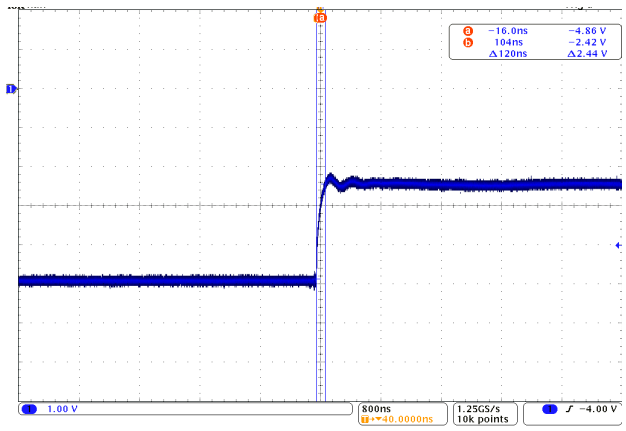
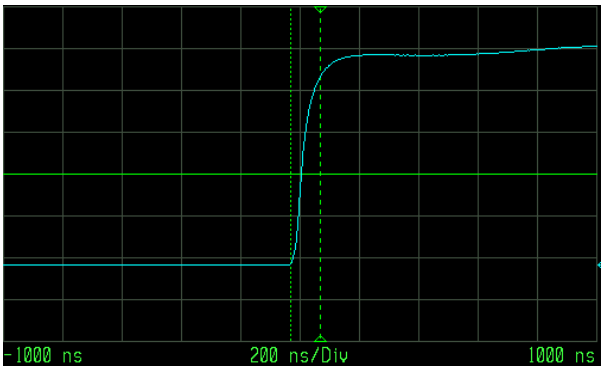


Fig. 4. Gate voltage waveform.



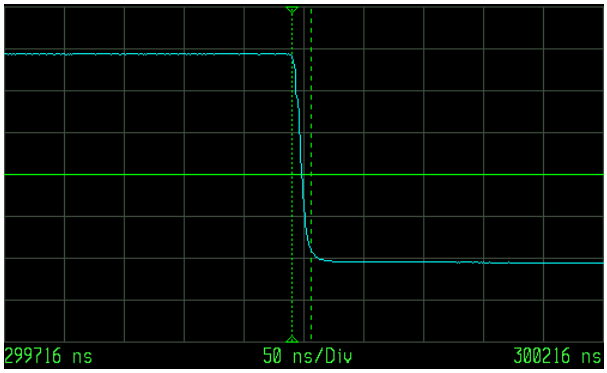


Fig. 5. Rise and Fall times of gate pulsing circuit..

IV. TEMPERATURE COMPENSATION

A temperature compensation circuit can be used to maintain a constant I_{dq}. A typical implementation is shown in Figure 6, where the temperature-dependent base-emitter voltage of PNP transistor MMBT2907 is used to generate the compensating voltage. Figure 7 shows gate voltage vs. temperature (for constant Idq) for Integra GaN transistor IGN1214M500. Approximately +0.6 mV/°C gate voltage compensation is required for this transistor.

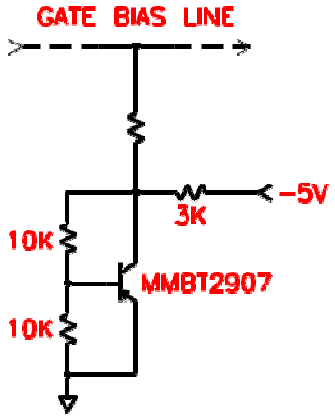


Fig. 6. Temperature Compensation Circuit.

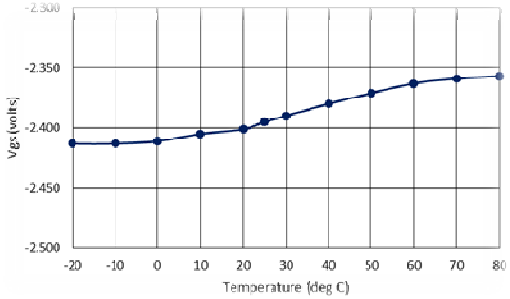


Figure 7: Vgs vs. temperature for constant Idq.

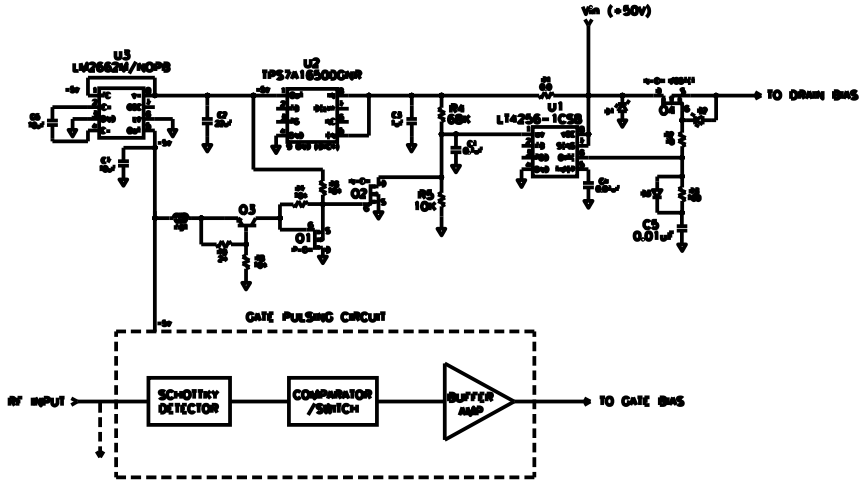


Figure 3. Schematic of Gate Pulsing and Sequencing Circuit

V. Conclusions

The necessity of using gate or drain pulsing for kW-level GaN transistors used in radar and avionic systems has been demonstrated. A novel fully automatic gate pulsing and sequencing circuit has been described that reduces the drain current in the pulse-off period to just the transistor leakage current. Measurements have been presented that show this circuit has typically 100ns and 16ns rise and fall times, respectively, with a pulse latency of 10ns. Using this circuit the efficiency over all time is typically just 0.4% less than the intrinsic transistor efficiency during the pulse for a 1kW transistor (the gate pulsing circuit consumes <1W i.e. it degrades efficiency by 0.1% while the MOSFET switch in the drain degrades the efficiency by 0.3%). The measured output noise has been suppressed by >30dB. Finally, a method of providing temperature compensation has been discussed.

References

[1] http://www.integratech.com/ProductDoc.ashx?Id=1233

[2] http://www.integratech.com/ProductDoc.ashx?Id=1240

[3] J. Millman, and C.C. Halkias, *Electronic Devices and Circuits*, New York: McGraw-Hill, 1967, p475.

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