A High-Performance 34 to 40 GHz Frequency Quadrupler Fabricated with Flip-Chip Technology

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Abstract **— A rugged flip-chip technology with potential for low cost at high manufacturing volume was employed to fabricate on a single substrate a frequency-quadrupling LO chain that had previously required a total of twelve wire-bonded chips in MMIC technology. A four-to-one reduction in the number of bond wires was achieved. Measurements on a typical circuit showed an output power of 17 ± 1 dBm over an output frequency range of 34 to 40 GHz and an input power range of 1 to 19 dBm. Spurious signal power was under -23 dBm. Self-regulating biasing with built-in bypassing simplifies the unit's application.**

Index Terms **— Millimeter wave frequency conversion, multichip modules, frequency conversion, millimeter wave integrated circuits, integrated circuit design, flip-chip devices.**

I. Introduction

As part of an effort to reduce costs and simplify millimeter-wave circuitry for mass production, an MLMS™ (MultiLithic MicroSystem™) technology has been applied to a multiplying LO (local oscillator) chain that had previously been implemented in MMIC (monolithic microwave integrated circuit) technology. Excellent performance results were achieved along with a dramatic simplification of the overall subsystem.

II. The Technology

In MLMS™ technology small semiconductor dice containing the active elements are flip-attached by way of an automated assembly process to an inexpensive substrate that contains all of the passive elements of the circuit. The attachment is achieved by thermocompression welding of the pads on the semiconductor dice to 30-micron-diameter gold bumps on the substrate—the same metallurgy as in wire bonding. These assemblies withstand repeated cycling between liquid nitrogen and a 300 ºC hot plate and repeated cycling between freezing and boiling while under water. They have been tested under mechanical shock at 3000 Gs, and, based on measured die pull forces, are expected to withstand 100,000 Gs.

The MLMS™ substrate, a cross-section of which is shown conceptually in Fig. 1, has built into it high-thermal-conductivity pedestals that are precisely shaped to thermally ground a bump while maintaining electrical isolation to other bumps spaced as little as 65 microns away center-to-center. Consequently, each flip-attached die can be less than 0.3 mm by 0.3 mm square in size and can have a thermal resistance equal to that of a 100-micron-thick die backside-attached eutectically to a heat sink.

Two other circuits fabricated in this technology [1]-[2] are being reported in 2006.

III. The Quadrupler Design

The MLMS™ quadrupler chip, shown in Fig. 2, consists of a 3.8 mm by 4.5 mm substrate with seven active PHEMT (pseudomorphic high-electron-mobility transistor) dice attached to it. One additional die used for quality control

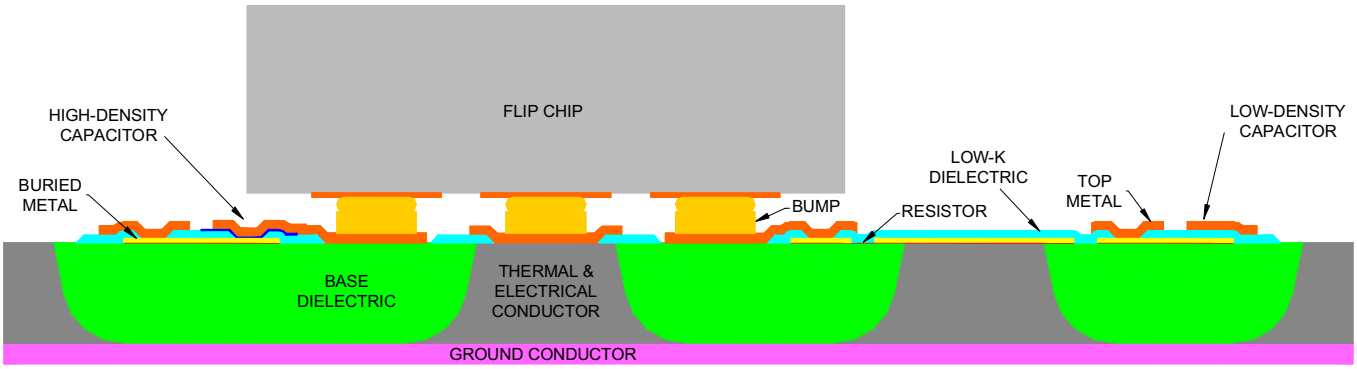

Fig. 1. Conceptual cross-section of a semiconductor die flip-attached to a passive integrated circuit. Multiple chips of various kinds can be flip-attached to a single substrate to produce a highly-integrated MLMS™ circuit.

purposes is also attached. Fig. 3 shows the block diagram. There are two active doublers, a filter, three single-transistor feedback-enhanced amplifiers, and a balanced power amplifier. The drain bias for all stages comes from a single +4 V pad and is dropped to +3 V by a resistor on each PHEMT drain line. The drain voltage on each PHEMT is fed back to the gate through a voltage divider to stabilize the bias on each stage. A -5 V pad connects to the negative sides of these dividers. The bias lines are individually filtered on the passive substrate, and a 22-picofarad capacitor is situated near each bias pad to bypass any remaining signal power to ground and to stabilize the circuit against low-frequency oscillation.

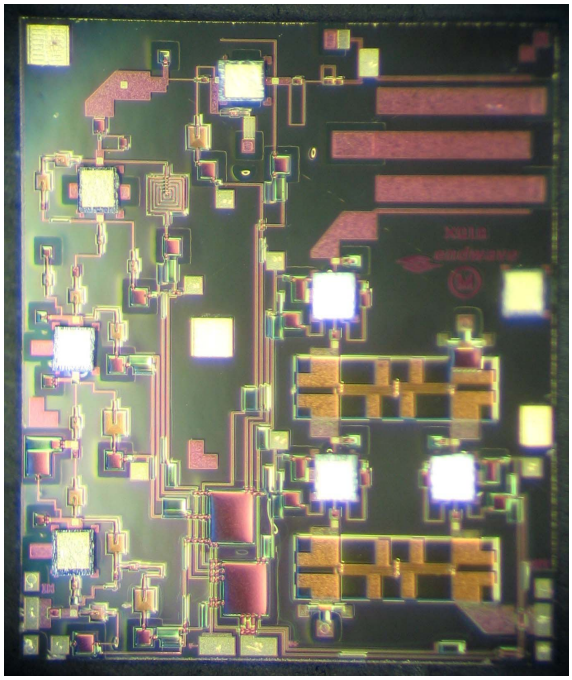

Fig. 2. Assembled quadrupler chip.

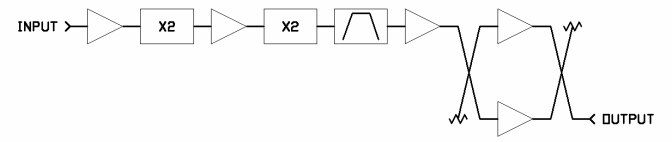

Fig. 3. Block diagram of the quadrupler.

IV. Results

Measurements of the performance of a typical quadrupler are shown in Fig. 4 and Fig. 5. With an input power level of 3 dBm and higher, the output power is saturated at 17 ± 1 dBm over the 34 to 40 GHz output frequency range. Over this same operating domain the strengths of the spurious output signals (at one, three, and five times the input frequency) are below -23 dBm. The minimum in-band input and output return losses derived from small-signal S-parameter measurements are 17.7 dB and 8.6 dB respectively.

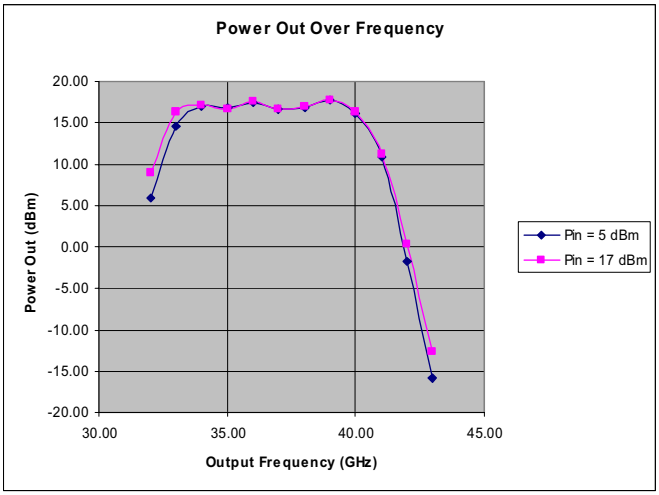

Fig. 4. Frequency response of the quadrupler at two RF input power levels.

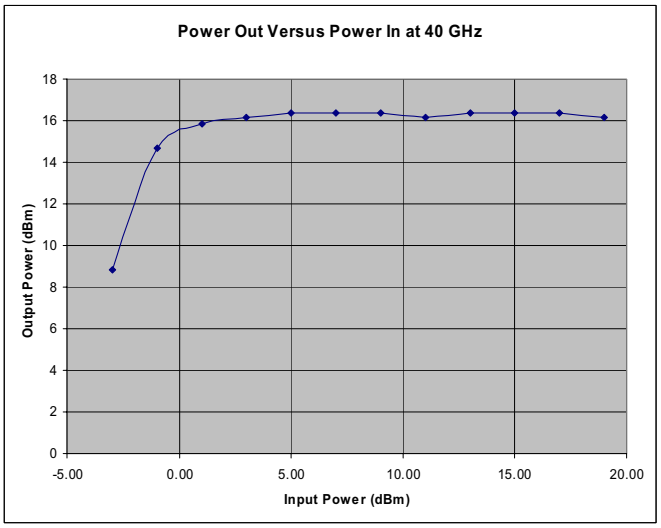

Fig. 5. RF output power at 40 GHz versus RF input power at 10 GHz.

Fig. 6 compares the MMIC implementation that had been previously required to achieve the above performance to the present MLMS™ implementation. The former employs an input modamp chip, a quadrupler MMIC, a post-amplifier MMIC, one filter substrate, 6 chip capacitors, 2 surface mount capacitors, and 29 bond wires. The latter requires only the MLMS™ circuit and 7 bond wires.

Unlike the MMICs used in the previous quadrupling LO chain implementation, the MLMS™ circuit requires no external bypass chip capacitors or bias-control circuitry. The DC feedback and RF bypassing on the MLMS™ substrate

make the unit stable enough to accommodate lengthy bondwires and traces in the path to the bias sources on a surface-mount printed-circuit motherboard. The biases can be taken from fixed-voltage regulators with standard tolerances and require no adjustments. In addition, the circuit does not require bias sequencing. The positive bias can be applied prior to the negative bias without causing overheating of the semiconductor devices.

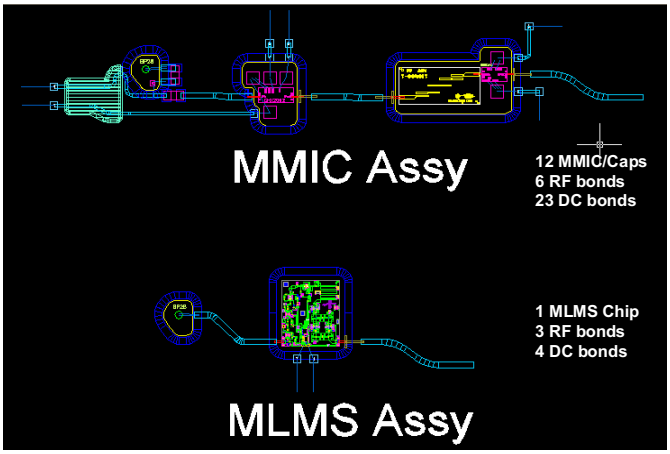

Fig. 6. Comparison of a quadrupling LO chain implemented with MMICs to one with matching performance implemented with MLMS™.

V. Conclusions

A technology that allows flip attachment of small active chips to a highly-integrated passive circuit substrate with built-in precision heat sinks has been utilized to simplify a frequency quadrupling LO chain while maintaining high performance. Multiple MMICs and other components are replaced with a single rugged multilithic integrated circuit offering the potential for substantial cost reduction. The high level of integration and the incorporation of bias conditioning within the circuit results in improved ease of use and a reduction in the cost of support circuitry.

Acknowledgement

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References

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