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Introduction

As wireless connectivity continues the evolution towards becoming one of the core utilities in our daily lives, the demand for increasing performance and ease of integration into consumer and industrial products drives the RF front end industry. Demand for RF front ends in consumer devices alone doubles from three to six billion units during the next three years. The semiconductor technologies used to manufacture RF front ends in such volumes play a critical part in enabling – or limiting – the pervasiveness of wireless connectivity as broadband multimedia redefines wireless communications networks.

Will GaAs, BiCMOS or CMOS be the technology of choice for future RF front ends and power amplifiers? Silicon BiCMOS proves to be the winner by offering performance, cost, and functional integration.

Silicon BiCMOS The Optimal Technology for RF Power

The debate over GaAs versus CMOS has been reinvigorated by recent industry events. This includes the sale of CMOS cellular power amplifier (PA) house Axiom Microdevices to GaAs cellular PA manufacturer Skyworks as well as the emergence from “stealth mode” of CMOS cellular PA startups Black Sand Technologies and Javelin Semiconductor. In terms of market share, since TRW Semiconductor paired with RF Micro Devices in the mid-to-late 1990s, the GaAs heterojunction bipolar transistor (HBT) has been the standard bearer for mobile phone PA performance, cost, and manufacturability. GaAs houses that design, manufacture and package their own PAs and other RF components dominate today’s cellular power amplifier market.

However, as has been the case in the semiconductor industry since its inception, all roads lead to silicon because it repeatedly proves to offer the optimal combination of performance, cost, functional integration, and manufacturability for digital and analog integrated circuits. Historically, RF circuitry has not been integrated in silicon. However, over the last two decades, the RF transceiver function has joined digital signal processing in silicon-based technologies. As a result, the RF PA and RF front-end system remain the last footholds for GaAs in the modern wireless communications device’s signal processing chain.

Design of RF front ends into foundry silicon technology would enable the third wave of the fabless revolution, which started with digital ICs, moved to analog, and finally RF/optical components. The fabless revolution will enable the RF industry to have the scale and supply chain to make multi-function wireless connectivity blocks truly ubiquitous.

Market Pressures for Silicon Technology

Wireless connectivity has become a standard product feature across the consumer electronics industry. What began with mobile phones, Bluetooth, and computer wireless LANs (WLAN, or WI-FI™) has expanded into wireless connectivity for everything from vending machines to televisions and digital cameras.

As Figure 1 shows, shipments of RF PAs and RF front ends for consumer electronics applications are expected to continue to grow at better than 21% per year from 2009 through 2013. With the existing GaAs fab capacity – captive and foundry – at or near maximum utilization, a critical question must be answered: does continuing growth in wireless connectivity

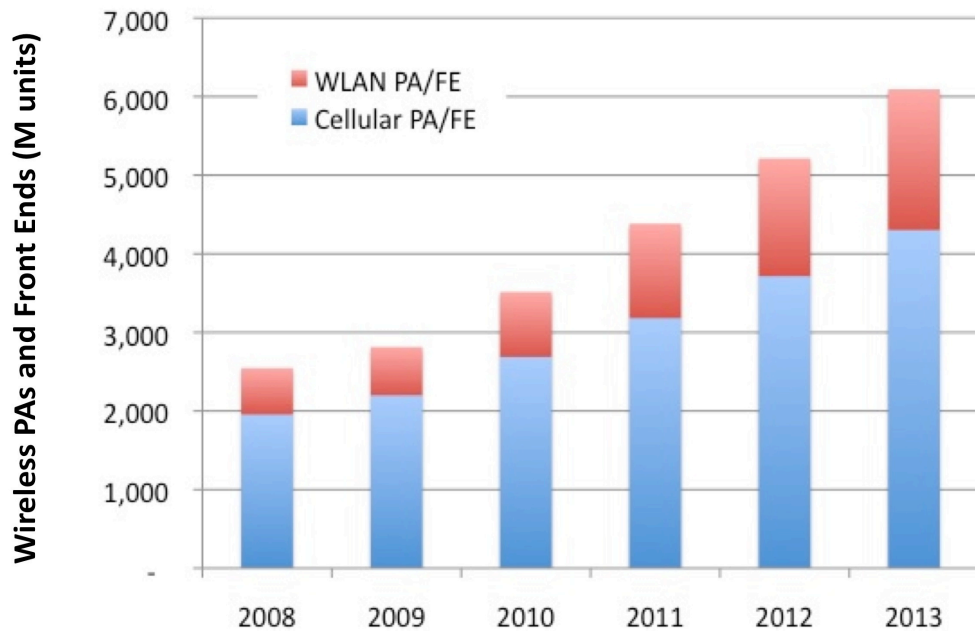


Figure 1: Dramatic growth in the demand for RF power amplifiers (PAs) and front-ends results from a combination of the rapid expansion of wireless connectivity in consumer electronics and the proliferation of multiple RF bands used worldwide for various wireless communications technologies.

Data: Strategy Analytics, August 2009

demand new GaAs fabrication facilities, or is the vastly larger worldwide silicon-based foundry capacity ready to expand into RF PAs?

It turns out this question has already been answered. Blending the best of the GaAs and CMOS advantages, silicon-based BiCMOS has proven itself to be the optimal technology for RF PAs and front ends in Wi-Fi. And, as wireless connectivity migrates to orthogonal frequency division multiplexing (OFDM), silicon-based BiCMOS becomes the leading technology for cellular, WiMAX, and Wi-Fi RF front-end systems. Silicon-based BiCMOS can leverage the world's silicon foundry capacity and respond to the market demand for ongoing integration of wireless connectivity into our daily lives.

Silicon BiCMOS Technology

So, what is BiCMOS technology, and why doesn't it receive the prominence and attention of either GaAs or CMOS in the RF PA technology debate?

BiCMOS is a combination of silicon CMOS and silicon-germanium graded base bipolar transistors on a single substrate. For RF applications, BiCMOS technology uses germanium doping of the silicon HBT base to increase switching speed and current gain with the additional of as few as three masking layers above a standard CMOS process flow. Because of its high f_T , BiCMOS has always been the technology of choice for high speed analog functions. The resulting SiGe HBT is used for RF amplifier and signal detection functions while the silicon CMOS is used for bias and control functions for the signal processing blocks (PA, LNA, etc.). Because RF front ends require relatively small digital blocks, the CMOS can be kept at a trailing technology node to reduce cost.

In this way, SiGe BiCMOS combines the RF performance typically achieved with a GaAs HBT with the cost and functional integration benefits of CMOS into a single technology. This approach drives down cost and improves performance in RF front ends, enabling wireless connectivity in the most cost-sensitive consumer applications.

Widely available from major foundries in the US (IBM, TowerJazz), Europe (STMicro), and Asia Pacific (TSMC, CSM, ASMC, Hua Hong NEC), foundry BiCMOS technology already has the capacity to support the volume demands of current and emerging wireless connectivity applications. In fact, any single BiCMOS process line can already support the current worldwide demand for RF front ends.

Validating the Process Technology

Comparing various transistor performance parameters, parametric device yields, or the cost benefits of 200mm BiCMOS wafers over 150mm GaAs wafers might be an interesting exercise for examining the viability of SiGe BiCMOS as a replacement for GaAs HBT in the RF PA market. But there's a much simpler way to validate the viability of SiGe BiCMOS. The decade-long relationship between SiGe Semiconductor (Andover, MA) and IBM Microelectronics (Burlington, VT) has provided the foundation from which SiGe Semiconductor has replaced GaAs HBT with SiGe BiCMOS in Wi-Fi RF front ends. (Of the 500M RF power amplifiers and RF front-end solutions

SiGe Semi has shipped, about 400M units have been manufactured using wafers processed by IBM.)

With SiGe Semiconductor leading the Wi-Fi RF PA and front-end industry, SiGe BiCMOS has a 35% market share position, confirming its viability in RF power applications. From discrete 2.4 GHz PAs to dual-band 2.4/5 GHz PA/LNA/RF switch single-die RF front ends, from +16dBm of RF power at 2.4GHz to +26dBm at 5 GHz, BiCMOS is proving that it can deliver all the performance of GaAs HBT at the cost and yield of silicon.

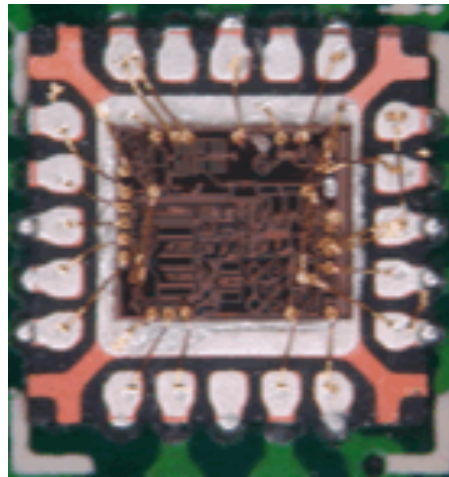


Figure 2: Example of a SiGe BiCMOS 2.4 GHz Front End IC incorporating Wi-Fi RF PA, Receiver LNA and RF switch enabling Bluetooth/Wi-Fi antenna sharing

Source: SiGe Semiconductor

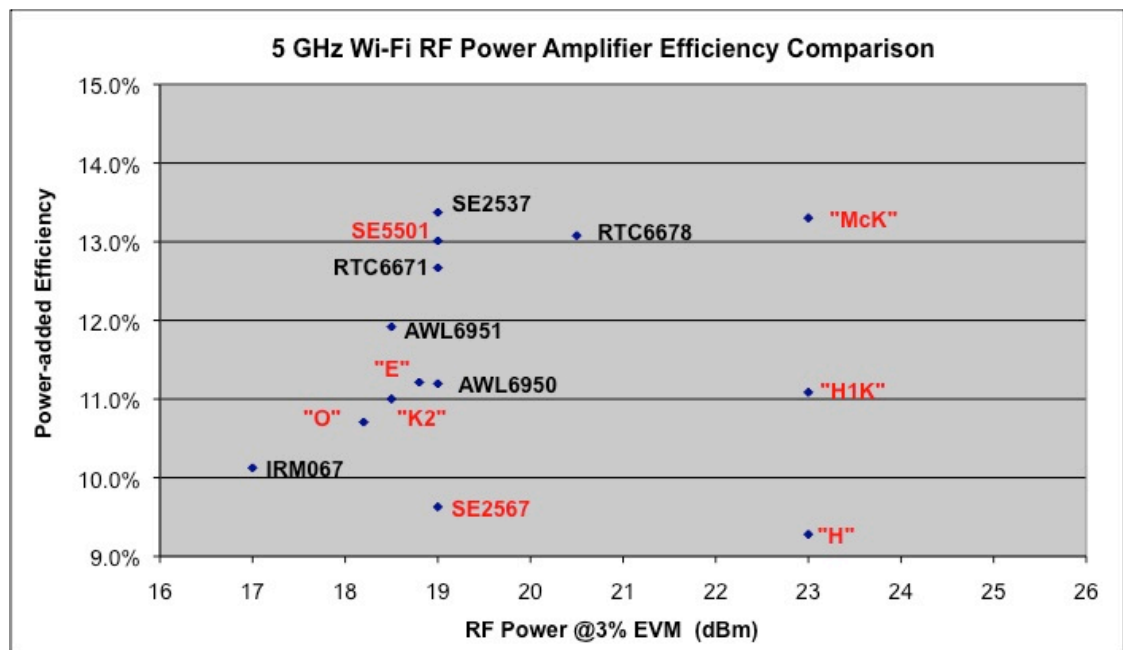
Head to Head: Performance

Will BiCMOS or CMOS be the technology of choice for future RF PAs? Both technologies leverage the benefits of silicon – superior thermal conductivity (important when PAs create more heat energy than RF energy in OFDM-based wireless communications), large-format wafers, low defect density, and an existing worldwide foundry capacity capable of supporting RF PA needs into the foreseeable future. The answer to this question lies with the same product features that have always separated the winners from the losers in RF power amplifiers for consumer electronics: performance, cost, and functional integration.

Performance is where BiCMOS RF power amplifiers distinguish themselves from CMOS PAs. Both CMOS and BiCMOS technologies are well-suited to

digital predistortion, calibration lookup tables, and other techniques for improving RF performance. However, the state-of-the-art in CMOS PA architecture continues to require significant compromises in wireless connectivity performance.

For example, while both process technologies offer roughly the same RF power per unit area capability, the nature of the lateral CMOS devices drives RF power amplifier architecture down a very different path than the traditional PA architectures to which HBTs are suited. Due to the substantial AM-PM peaking, low breakdown voltage and low current gain of the CMOS device, a CMOS RF PA must rely heavily on multiple stacked devices and large, high-Q inductors for impedance transformation to 50 ohms, harmonic suppression, and voltage transformation to achieve the required RF power levels. Using these techniques, CMOS PAs have proven themselves capable of cellular RF power levels in the +26-33dBm range for 2G applications and CMOS devices with Wi-Fi RF power levels of +10-15dBm have been mass produced. However, because of the inherent nonlinearities of CMOS PAs



GaAs discrete PAs

BiCMOS discrete PAs (including discrete PA die used in RF front end solutions, names in quotation marks)

Figure 3: Comparison of SiGe and GaAs Wi-Fi Power Amplifier Efficiency performance across a range of maximum RF output power levels

and lower Q of passive components, none to date have achieved the efficiency or linearity levels of BiCMOS HBT-based designs in Wi-Fi applications, which typically demonstrate 18% efficiency in the 2.4 GHz band and 11% in the 5 GHz band.

Multimedia applications for Wi-Fi demand increases in RF power for ensuring first-time delivery of real-time data such as voice over Internet Protocol (VoIP) and streaming video for home-entertainment systems. As Wi-Fi RF power levels reach into the same +23-26 dBm power range used in 3G cellular systems, PA operating efficiency takes on a higher level of importance than in relatively low-power non-real-time use such as wireless printing. The 5 GHz Wi-Fi band plays a critical role in enabling high-bandwidth wireless multimedia applications. While SiGe BiCMOS RF front ends (for example, the SiGe Semiconductor SE2576) have already established performance parity with GaAs in the +26 dBm range at 2.4 GHz, recent developments show significant improvements in RF power from BiCMOS at 5 GHz (see Figure 3). SiGe BiCMOS-based RF front ends coming to market over the next 12 months achieve both RF power and efficiency parity in the 5 GHz Wi-Fi band with GaAs devices.

Examining Real Costs

One advantage touted by the CMOS PA proponents is the potential cost benefits of using bulk CMOS for RF PA applications, which some claim outweigh any shortcomings in performance for consumer-electronics applications. However, a closer study of the cost of the CMOS technologies that need to be used for RF PAs contradicts this assumption.

The latest PA architectures in the linear CMOS PA field use process technology nodes ranging from 90 to 180 nm. The inductors critical to these architectures handle very high currents and, as such, require the use of 8 to 10 metal layers for their construction. Let's put some numbers to this. CMOS processes designed for digital microprocessor manufacturing typically have 3 to 4 metal layers and, according to data from the Global Semiconductor Alliance, on the 0.18 micron 200mm wafer technology node, currently cost about \$700 in mass production quantities. However, 0.18 micron 200mm wafers with 8 metal layers averaged \$1250 during 1Q2010.

In comparison, 0.18 micron 200mm BiCMOS wafers with 4 metal layers averaged \$1750 during 1Q2010 – a 40% premium in cost with respect to CMOS. However, due to the size of the inductors in the on-chip

transformer, a CMOS PA die is about twice the area of a BiCMOS PA for a given set of performance specifications. In addition, the manufacturing yield for SiGe BiCMOS is well in excess of 90%. Combining these considerations, it's easy to conclude that RF power CMOS and BiCMOS process technologies have the same die-level cost profiles for RF PAs.

Functional Integration

Once performance and cost advantages are dismissed, the remaining value proposition for the CMOS PA is the promise of a single-chip wireless connectivity solution: a single-chip mobile phone, a single-chip Wi-Fi or WiMAX modem.

And single-chip Wi-Fi modems – generating +10 to +15 dBm of RF power in 2.4 GHz 802.11b/g/n applications – have been shipping in mass production quantities for almost a year. Useful in cost-sensitive USB dongles, netbooks and printers, these so-called “integrated PAs” are aimed at low-end performance requirements and are expected to make up about 25% of all the Wi-Fi RF PAs shipped in 2012. Top wireless connectivity chipset providers such as Intel, Samsung, and Broadcom are leading the effort to integrate the PA for segments of the cellular and Wi-Fi markets where solution cost outweighs all other requirements. Despite a general industry perception to the contrary, the integrated CMOS PA is real, and it will be a contributor to the expansion in wireless connectivity in consumer electronics.

A primary difference between the value of CMOS for digital systems and for RF power amplifiers lies with the value of Moore's Law to each application. In digital systems such as microprocessors, transistor speed and power consumption are the primary design goals at the semiconductor technology level. Smaller transistors switch faster for a given bias current; hence, increases in microprocessor speed rely upon continuing decreases in CMOS device geometry. In the RF realm, the world's spectrum regulators (government bodies like the US Federal Communications Commission and non-government bodies like the International Telecommunications Union) define the speeds at which the RF power amplifier must operate. Beyond that speed, there is no benefit from Moore's Law in RF power applications.

In fact, Moore's Law indirectly poses a challenge for the single-chip wireless connectivity solution model. While digital microprocessors benefit greatly in performance and cost from reduction in CMOS device geometry, RF power

amplifiers suffer from it. Both breakdown voltage and current gain decrease with shrinking CMOS device geometry. As such, CMOS PA architectures valid for process technology nodes in the 90 to 180 nm range do not transfer to lower geometry process nodes. This means that the last decade of work on CMOS PA architectures, focused primarily on the 130 and 180 nm process nodes, must be reworked if the integrated CMOS PA is going to migrate along with the microprocessor to 45 nm and below. Alternatively, this means that wireless connectivity signal processing solutions cannot migrate below the 90 nm node if they are to include an integrated PA. If integrated CMOS PAs are part of the wireless connectivity technology roadmap, the industry will have to accept a hard limit on microprocessor functionality, performance, and cost.

If the single-chip wireless connectivity solution appears impractical, a two-chip variant seems to deliver on the promise of all-CMOS wireless connectivity. By merging the PA with the RF transceiver in a separate die at the 90 nm process node, the stand-alone microprocessor continues to benefit from advances in CMOS device geometry. And, given that the combination of CMOS PA and transceiver die area is approximately 25% of the microprocessor, leaving the RF portion of the wireless connectivity solution at 90 nm has only an incremental cost disadvantage against the single-chip approach. The two-chip CMOS solution is being implemented for the Wi-Fi market, and it will ship into low-end computing products beginning this year. Focus on the cost-sensitive lower performance segment of Wi-Fi is expected to be the primary product model for integrated CMOS PAs. The requirement for efficient high-power RF PAs in multimedia wireless connectivity drives this two-chip solution to a combination of BiCMOS for the RF portion and CMOS for the microprocessor.

For wireless connectivity, the optimal blend of RF PA and front end performance, cost, and functional integration points to silicon-based BiCMOS technology. When maximum quality of data transport over the widest possible coverage area is the goal (for voice, mobile, and enterprise data or in-home video distribution), BiCMOS provides high performance (comparable to GaAs) with CMOS cost and functional integration. And, as fixed and mobile voice and data networks converge through OFDM, the rich history of BiCMOS in 802.11a/b/g/n applications extends directly into the full range of 4G devices, including the main communications path in mobile phones. For the present and future of wireless connectivity in consumer electronics, then, the answer to the question “GaAs or CMOS?” is BiCMOS.

Authors



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John has served as our Vice President, Corporate and Business Development since October 2007 and was previously our Vice President, Marketing from April 2006 to October 2007. Prior to joining us, he was chief executive officer, president and a member of the board of directors of Xindium Technologies, Inc., a company providing RF power amplifiers for next-generation mobile handsets and terminals, from 2003 to 2005 where he focused on business development, marketing and sales. From 2000 to 2003, John worked at Vincio LLC and from 1997 to 2000, at Tropian, Inc. he successfully grew wireless transceiver product lines in management positions at SEIKO Communications Systems, Inc. from 1995 to 1997, Analog Devices, Inc. from 1994 to 1995 and Tektronix, Inc. from 1990 to 1994. He holds a Bachelor of Science degree in electrical engineering from Santa Clara University.



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Peter has served as our Chief Technology Officer and Vice President, Engineering since June 2007. Prior to joining us, he served as vice president, engineering at Renaissance Wireless Corporation, a venture-backed startup, from August 2006 to 2007 where he assembled and managed a 15-person team to develop RF acoustic wave products. From 2005 to 2006, Peter was the chief technology officer at Advance Nanotech, Inc., a development-stage company specializing in the commercialization of nanotechnology, where he developed and managed an early stage development fund for a publicly traded company. From 2000 to 2005, he worked at Agere Systems, Inc. (acquired by LSI Logic Corporation), where he was chief technology officer in the analogue products business unit from 2002 to 2005 and director, MEMS research from 2000 to 2002. From 1986 to 2000, Peter was a research director at Bell Laboratories, a research and development organization of Alcatel-Lucent. He holds a PhD in physics from Cornell University and Bachelor of Science degrees in physics and mathematics from Massachusetts Institute of Technology.