Normalized Phase Noise in UltraCMOS™ Devices

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What is Phase Noise?

Phase Noise is a measure of the spectral purity of a signal in an oscillator system. It quantifies the short-term random variation of the frequency of the signal, and is a product of thermal noise and low frequency flicker noise injected into the oscillator. Most RF systems require an overall integrated phase noise specification to be met, as phase noise can corrupt both the upconverted and downconverted signal paths. For digital systems, the integrated phase noise can be converted and expressed as phase jitter.

In the frequency domain, phase noise is typically quantified at various frequency offsets from the carrier frequency. Expressed as a ratio in units of dBc/Hz, the noise power in a 1 Hz bandwidth is measured at each offset frequency and divided into the carrier power. If noise sidebands on either side of the carrier are measured, the phase noise at each offset can be expressed as a double-sideband value instead of a single-sideband value.

Phase Noise in PLL Frequency synthesizers

A frequency synthesizer is used to generate multiple output frequencies from a single reference frequency. Used in a Phase-Locked Loop (PLL), a divided down output can be compared to a scaled reference, generating an error signal that drives the loop to achieve both frequency and phase lock (*Fig. 1*).

Phased-Locked Loop (PLL) phase noise is shaped by several noise contributors including 1/f noise, reference noise, phase detector noise, and VCO noise. The loop bandwidth defines the range over which the output tracks the input. Within the loop bandwidth, the phase detector drives the VCO to track the reference. In this process, the phase detector noise floor dominates the overall phase noise. At very large-frequency offsets, the loop does not track the reference and the PLL noise is set by the VCO phase noise. Ideally, the PLL loop bandwidth is designed so that the phase detector noise floor crosses the free-running VCO noise.

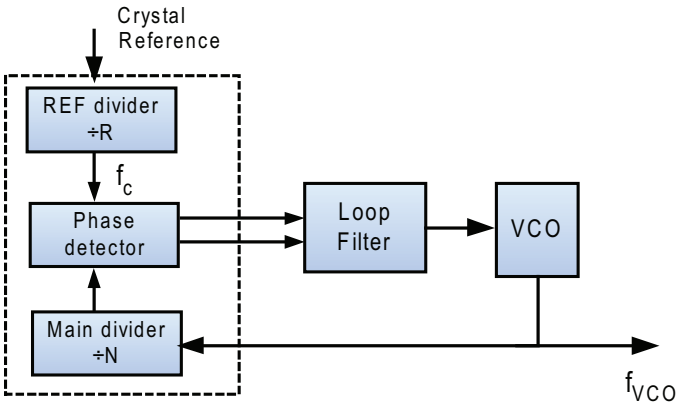

Figure 1. Block Diagram of PLL Frequency Synthesizer

Normalized Phase Noise

Peregrine Semiconductor uses normalized phase noise as the benchmark specification for its PLL products. Normalized phase noise is a handy single figure of merit that can be used to evaluate the phase noise performance of the PLL. By normalizing the phase detector noise floor to 1 Hz, the In-loop phase noise (dominated by the phase detector) can be easily calculated for any comparison frequency and VCO frequency as follows:

PD Phase Noise (dBc/Hz) =
Normalized Phase Detector Noise Floor (dBc/Hz)
+ 10log(f_c) + 20log(N),
where
f_c = comparison frequency
f_{vco} = VCO output frequency
N = f_{vco}/f_c

Take for example, the PE97022 3.5 GHz Integer-N PLL synthesizer for space applications. The standard reference design at 1920 MHz can be used to calculate the PD Phase Noise as follows:

With f_{vco} = 1.92 GHz and f_c = 20 MHz
PD Phase Noise (dBc/Hz) = -216 dBc/Hz +
10log(20e6) + 20log(1.92e9/20e6)
= -103.4 dBc/Hz

Fig. 2 shows the measured typical Phase Noise for the standard reference design.

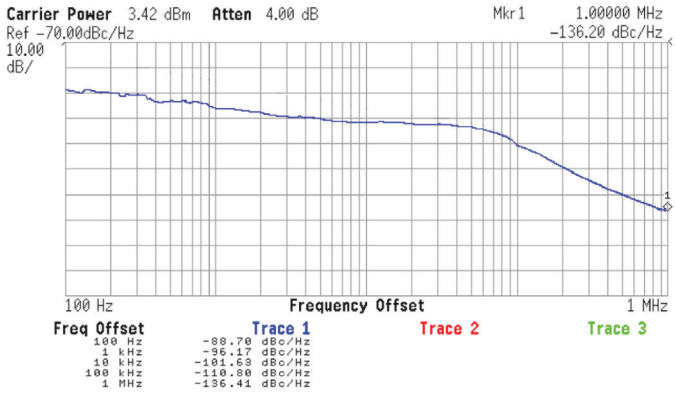

Figure 2. Typical Phase Noise for PE97022, VDD = 3.3 V, Temp = 25 C, f_{vco} = 1.92 GHz, Fcomp = 20 MHz, Loop Bandwidth = 50 kHz

Observing the plot at a frequency offset in the flat portion of the loop (30 kHz), the phase noise value is very close to the the calculated value. At this point in the loop, the 1/f noise has rolled off and the PD noise is the dominant noise contributor.

The PD phase noise can be reduced by 3 dB by doubling the comparison frequency:

With f_{vco} = 1.92 GHz and f_c = 40 MHz, the PD Phase Noise can be calculated as

PD Phase Noise (dBc/Hz) = -216 dBc/Hz +
10log(40e6) + 20log(1.92e9/40e6)
= -106.4 dBc/Hz

In this fashion, the user can easily determine if the PLL can meet the overall Phase Noise requirements.

Reference:
Peregrine Semiconductor Application Note 16:
"Using Peregrine Phase-Locked Loop Integrated Circuits in Reference and System Clock Applications."

http://www.psemi.com/pdf/app_notes/an16.pdf